A NOVEL HEAT DISSIPATION STRUCTURE WITH EMBEDDED BOTH THROUGH SILICON VIAS AND MICRO-CHANNELS FOR IMPROVING HEAT TRANSFER PERFORMANCE OF THREE-DIMENSIONAL INTEGRATED CIRCUITS

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This paper proposed a new heat dissipation structure with embedded both through silicon vias (TSVs) and micro-channels to solve the complex heat problems of three-dimensional integrated circuits (3D-ICs). The COMSOL simulation model is established to investigate the characteristics of steady-state response for the defined four cases. The simulation results show that our proposed heat dissipation structure (i.e., case 4: 3D-ICs with embedded both TSVs and micro-channels) can reduce steady-state temperature over 43.546%, 18.440% and 12.338% in comparison to case 1 (i.e., 3D-ICs without embedded heat dissipation structure), case 2 (i.e., 3D-ICs with only inserted TSVs) and case 3 (i.e., 3D-ICs with only embedded micro-channels), respectively. Besides, it is demonstrated that CNTs as filler material of TSVs and CNTs nanofluid as coolant of micro-channels (i.e., the proposed scheme 4) can further reduce steady-state temperature of 3D-ICs with embedded our proposed heat dissipation structure. The corresponding results illustrated that the steady-state temperature of scheme 4 is reduced by 13.767% as compared with scheme 1 (i.e., the conventional Cu as filler material of TSVs and water as coolant of micro-channels). Moreover, it is manifested that the heat transfer performance of 3D-ICs with embedded the proposed heat dissipation structure can be enhanced by the increase of TSVs radius and flow rate of coolant of micro-channels. Therefore, our proposed heat dissipation structure has great prospect for enhancing heat transfer performance of 3D-ICs.

Key words*: three-dimensional integrated circuits; heat dissipation structure; heat transfer performance.*

1. Introduction

The advent of 3D-ICs has given a great impetus to development of semiconductor integrated circuit, which expand the conventional two dimensional integrated circuits (2D-ICs) into three dimensional space by stacking multiple chips in the vertical direction [1–3]. The 3D-ICs can evidently reduce interconnect length, power consumption and propagation delay as compared with 2D-ICs [4–6].

However, the power density of 3D-ICs will be increased due to the continuously rising of operation frequency and the increasing number of stacked chips in the vertical direction, which results in forming the excessive temperature rise of 3D-ICs [7–9]. Hence, it is imperative to improve heat transfer performance for solving the increasingly serious heat problems of 3D-ICs.

To date, the 3D-ICs with inserted TSVs in the vertical direction and embedded micro-channels in the silicon substrate are regarded as the two most common solutions for solving the complex heat problems of 3D-ICs. Since the filler material of TSVs (usually copper) possess the high thermal conductivity, thus the heat can be transferred from the multiple stacked dies to TSVs in the lateral direction, then can enable it to release from TSVs to the external ambient of 3D-ICs by heat sink and package in the vertical direction in time [10–12]. Generally, the micro-channels are embedded in per silicon substrate layer of 3D-ICs, and their interior are filled with the coolant. And the flow rate of coolant in micro-channels is depended on pump power and geometric dimensions of micro-channels. The heat is conveyed from the side walls of micro-channel into the coolant, then can be transferred along with the coolant into the outside ambient of 3D-ICs [13–16].

At present, there has been a multitude of researches for using TSVs or micro-channels as heat dissipation structures to cope with the extreme heat problems of 3D-ICs. Xiao *et al.* in ref. [17] investigated effects of physical parameters of TSVs on the heat transfer performance of 3D-ICs, meanwhile the equivalent thermal conductivity of 3D-ICs is obtained by using finite element analysis method. In ref. [18], Hou *et al.* proposed a novel structure of TSVs cluster and corresponding simulation results indicated that 3D-ICs with inserted novel TSVs cluster's structure can clearly enhance heat transfer performance of 3D-ICs. Zajac *et al.* in ref. [19] studied the heat transfer performance of 3D-ICs with embedded a single-layer micro-channel under different size of micro-channel by using COMSOL software. And the simulation results suggested that increasing the size of the micro-channels and pump power all can improve heat transfer performance of 3D-ICs, meanwhile it is also concluded that excessively increasing the size of micro-channels and pump power can result in diminishing returns of heat transfer performance. In ref. [20], Ali *et al.* analyzed heat transfer performance of different shapes of pillar micro-channels (i.e., triangular prism pillar micro-channels, rectangular pillar micro-channels and circular pillar micro-channels), and corresponding experimental results illustrated that the rectangular pillar micro-channels have better heat transfer performance than other pillar micro-channels at over high Reynolds number case. Song *et al.* in ref. [21] proposed an numerical model of 3D-ICs with embedded micro-channels, and corresponding results indicated that the 3D-ICs with embedded micro-channels scheme has prominent heat transfer performance. In ref. [22], the heat transfer performance for different physical parameters of micro-channels is investigated, and corresponding experimental results shown that the volume-average temperature rise decreases as the width of micro-channels increases. In ref. [23, 24], Roy and Qian *et al.* constructed two different thermal models by using COMSOL software for estimating heat transfer performance of 3D-ICs with inserted TSVs case and the 3D-ICs with embedded micro-channels case respectively, and simulation results suggested that 3D-ICs with embedded TSVs or micro-channels all can significantly improve heat transfer performance of 3D-ICs.

Based on the aforementioned discussions, it can be found that most studies with respect to heat dissipation structures of 3D-ICs are focused on the TSVs or micro-channels. There is no doubt that TSVs or micro-channels all can improve heat transfer performance of 3D-ICs. However, there are still some limitations for them to overcome the continuous increasing temperature rise of 3D-ICs in the practical thermal design. Hence, it is crucial that the chip designer ought to seek new structures with

better heat transfer performance to solve these heat problems of 3D-ICs. Based on the available literatures, till date few studies have investigated the heat transfer performance concerning the new structures of 3D-ICs with embedded both TSVs and micro-channels. Moreover, it should be noted that the presented results of this paper are not validated with the experimental model. The reason behind this is that the preparation and performance evaluation of 3D-ICs with integrated the proposed heat dissipation structure have strict requirements for the production and testing equipment. Therefore, the COMSOL simulation model regarding our proposed new heat dissipation structures of 3D-ICs with embedded both TSVs and micro-channels is established to analyze its heat transfer performance in this paper, which are compared with other heat dissipation structures (including case 1 (i.e., 3D-ICs without embedded heat dissipation structure), case 2 (i.e., 3D-ICs with only inserted TSVs) and case 3 (i.e., 3D-ICs with only embedded micro-channels)), respectively. Besides, for ensuring the rationality of simulation model, the effects of temperature on thermophysical properties of TSVs filler material and coolant of micro-channels are considered in the proposed simulation model.

In the practical application, the most widely filler material for TSVs and the most common coolant for micro-channels are copper (Cu) and water, respectively. In order to further improve heat transfer performance of our proposed heat dissipation structure, it is extremely vital to explore new filler material of TSVs and new coolant of micro-channels. In recent years, carbon nanotubes (CNTs) have captured intensive interest from many researchers owing to its excellent electrical and thermal characteristics. The thermal conductivity of CNTs can exceed 800 W/m·K, while the thermal conductivity for the conventional Cu is only 400 W/m·K at room temperature [25]. Hence, the CNTs is adopted as a promising candidate for replacing the conventional Cu as filler material of TSVs in this work. On the other hand, the thermal conductivity of water is only 0.61 W/m·K at room temperature, while the thermal conductivity for CNTs nanoparticles as nanofluid can reach to 5.3 W/m·K [26]. The nanofluid is the suspension of nanometer-sized materials that is composed of nanoparticles (usually including metals, oxides, or CNTs) and base fluid (usually including water or oil) in specific proportions [27, 28]. At present, the nanofluid has become a research hotspot for enhancing heat transfer performance of micro-channels in terms of its excellent thermal properties [29]. Based on the discussions mentioned above, the CNTs nanofluid as coolant of micro-channels for improving heat transfer performance of 3D-ICs with integrated our proposed heat dissipation structure is also investigated in this paper due to its high thermal conductivity.

To the best our knowledge, most studies concerning the heat dissipation structures in 3D-ICs are focused on the case 2 (i.e., 3D-ICs with only inserted TSVs) or case 3 (i.e., 3D-ICs with only embedded micro-channels). Meanwhile, it can be found that the Cu and water are the most widely filler material of TSVs and the most common coolant of micro-channels, respectively. Therefore, in order to verify the performance advantage of our proposed heat dissipation structure (i.e., 3D-ICs with embedded both TSVs and micro-channels), which are compared with the conventional case 2 and case 3 in this paper. Besides, the CNTs as filler material of TSVs and CNTs nanofluid as coolant of micro-channels for further improving heat transfer performance of the proposed heat dissipation structure are also investigated in this work. In addition, the main contributions of this work can be summarized as follows:

(1) The novel heat dissipation structure is proposed in this work for enhancing heat transfer performance of 3D-ICs.

(2) The CNTs are introduced as filler material of TSVs and nanoparticle of nanofluid to further reduce steady-state temperature of 3D-ICs.

(3) The impacts of the radius of TSVs and flow rate of coolant on heat transfer performance of 3D-ICs with integrated our proposed heat dissipation structure are investigated in this work.

2. Analytical method

The proposed heat dissipation structure regarding the 3D-ICs with embedded both TSVs and micro-channels are shown in Figure 1(d). In order to investigate the superiority of heat transfer performance for the proposed heat dissipation structure in 3D-ICs as compared with other conventional heat dissipation structure, the four cases concerning 3D-ICs with embedded different heat dissipation structures are defined as follow, case 1: 3D-ICs without embedded heat dissipation structure, case 2: 3D-ICs with only inserted TSVs, case 3: 3D-ICs with only embedded micro-channels, case 4: 3D-ICs with embedded both TSVs and micro-channels, which are exhibited in Figure 1 respectively. Here, the N-layers stacked chip for the defined four cases are bonded in type of face-to-back.

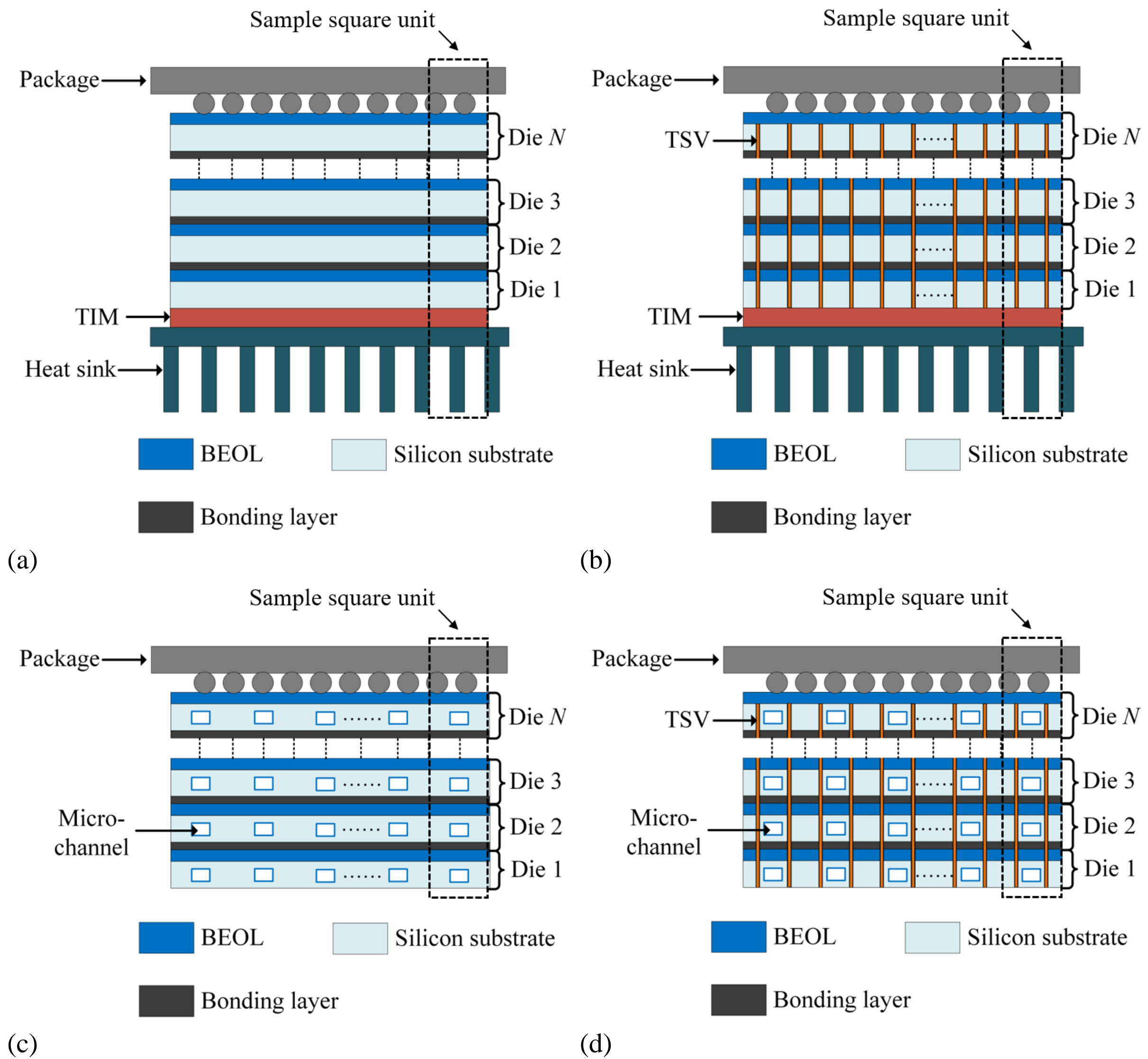
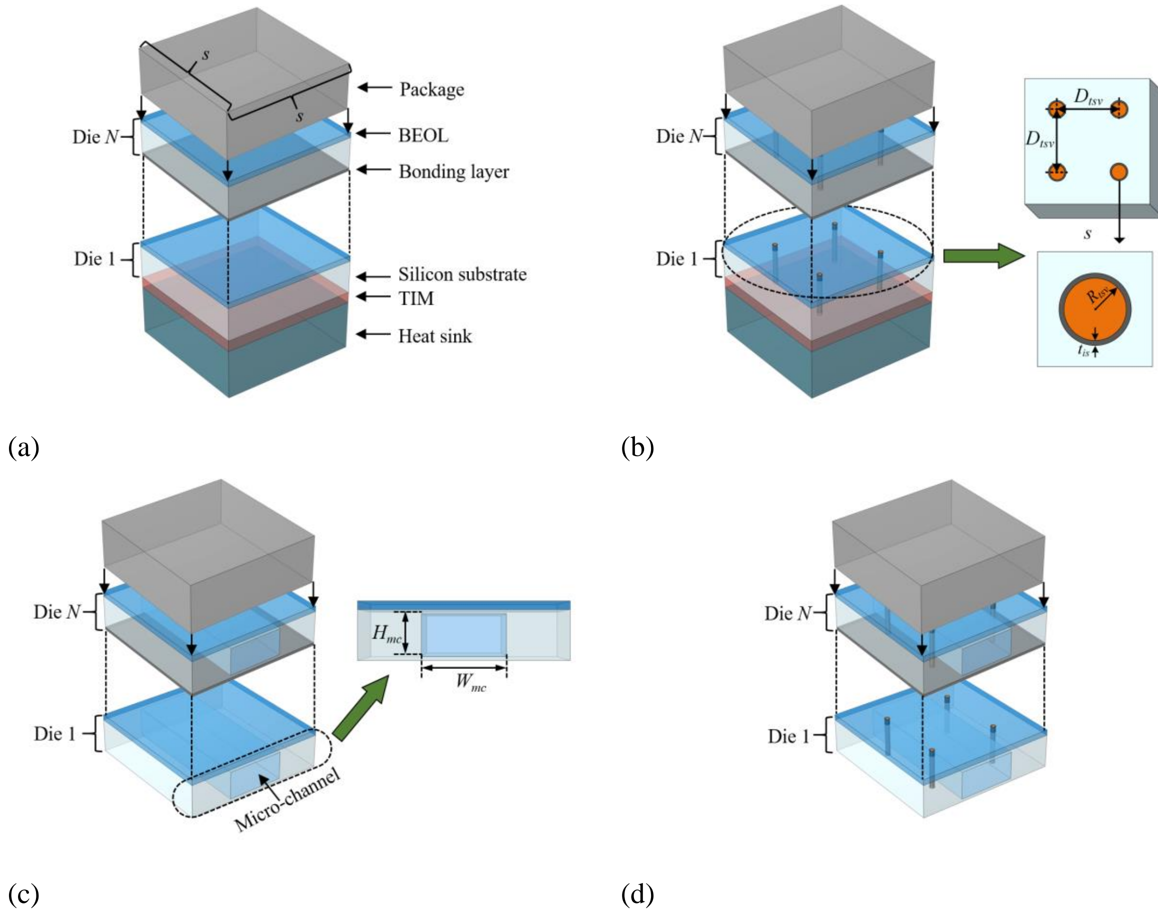


Figure 1. The cross-section diagram of the overall structure for 3D-ICs with embedded different heat dissipation structures: (a) 3D-ICs without embedded heat dissipation structure (i.e., case 1), (b) 3D-ICs with only inserted TSVs (i.e., case 2), (c) 3D-ICs with only embedded micro-channels (i.e., case 3), (d) 3D-ICs with embedded both TSVs and micro-channels (i.e., case 4).

As described in Figure 1(a) and Figure 1(b), the structures for case 1 and case 2 include package, back end of line (BEOL), silicon substrate, bonding layer, thermal interface material (TIM) and heat sink [2]. However, it can be seen from Figure 1(c) and Figure 1(d) that the TIM and heat sink were not integrated into the defined case 3 and case 4. These can be explained that the bottom surface of the defined case 3 and case 4 architectures need to provide electronic and photonic access [30, 31].

As shown in Figure 1(a), the heat generated by BEOL layer is transferred to the external ambient of chip via heat sink and package in the vertical direction for the case of 3D-ICs without embedded heat dissipation structure. The case 2 as displayed in Figure 1(b), the heat can be transferred by TSVs to the heat sink and package in vertical direction. The case 3 as described in Figure 1(c), the heat can be absorbed by coolant of micro-channels into the external ambient of 3D-ICs. Consequently, for our proposed case 4 (as shown in Figure 1(d)), the heat can be conveyed into the external ambient of 3D-ICs by the TSVs and micro-channels simultaneously.



(a) (b)

(c) (d)

Figure 2. The 3D view diagrams of sample square unit for 3D-ICs with embedded different heat dissipation structures: (a) 3D-ICs without embedded heat dissipation structure (i.e., case 1), (b) 3D-ICs with only inserted TSVs (i.e., case 2), (c) 3D-ICs with only embedded micro-channels (i.e., case 3), (d) 3D-ICs with embedded both TSVs and micro-channels (i.e., case 4).

In order to simplify the analysis, it is assumed for Figure 1 that the micro-channels are uniformly embedded in all silicon layer of 3D-ICs, meanwhile TSVs are evenly integrated in 3D-ICs in vertical direction. Since the 3D-ICs can be regarded as a uniform distribution structure with respect to TSVs and micro-channels, thus we can utilize the sample square unit to represent the performance of overall 3D-

ICs [32]. And the 3D view diagrams of sample square unit regarding the defined four cases are depicted in Figure 2. Especially, it ought to be pointed out for the case 4 that the micro-channels are evenly distributed in center of silicon substrate of sample square unit, and the columnar TSVs cluster are placed in both sides of micro-channels symmetrically. Herein, W_{mc} and H_{mc} are the width and height of micro-channel, respectively. The D_{tsv}, R_{tsv} and t_{is} denote the spacing of center to center of TSVs, TSVs radius and thickness of insulation medium (usually SiO_2), respectively. The s is the side length of sample square unit of 3D-ICs.

The analytical expression of solid heat transmission can be given as follows [33, 34],

$$C_v \frac{dT}{dt} + \left(-k\nabla^2 T\right) = q_v \tag{1}$$

Similarly, the analytical expression of heat transmission from solid to liquid can be defined as below [34],

$$C_v \frac{dT}{dt} + \nabla\left(-k\nabla T\right) + C_v u_v \nabla T = q_v \tag{2}$$

where, k and T represent the thermal conductivity of material and the temperature of material, q_v denotes the volumetric rate of heat generation of inside the BEOL layer of 3D-ICs and u_v represents the velocity of outflow of the fluid at the surface of the control volume. C_v is the volumetric specific heat capacity of material and its expression can be written as [35],

$$C_v = \rho C_p \tag{3}$$

here, ρ and C_p are the density and specific heat capacity of material, respectively.

In order to obtain more accurate calculation results, the effects of temperature on thermophysical properties of both TSVs filler material and coolant of micro-channels are considered in this paper. When the Cu is adopted as filler material of TSVs, the relationship between temperature and thermophysical properties of Cu can be formulated as follows (0 ℃ $\ll T \ll$ 100 ℃, 0 ℃ $\ll T_1 <$ 26.85 ℃ and 26.85 ℃ $\ll T_2 \ll$ 100 ℃) [36–39],

$$\begin{aligned} k_{cu}(T) = {} & 762.582657 - 5.70709974(T+273.15) + 0.0364306908(T+273.15)^2 \\ & -(1.20974465E-4)(T+273.15)^3 + (2.18735712E-7)(T+273.15)^4 \\ & -(2.04832488E-10)(T+273.15)^5 + (7.77997189E-14)(T+273.15)^6 \end{aligned} \tag{4}$$

$$\rho_{cu}(T) = 9062.242 - (3.913962E-1)(T+273.15) - (8.947644E-5)(T+273.15)^2 \tag{5}$$

$$\begin{aligned} C_{p,cu}(T_1) = {} & -215.281402 + 8.23639228(T_1+273.15) - (4.73210818E-2)(T_1+273.15)^2 \\ & +(1.29111169E-4)(T_1+273.15)^3 - (1.35703145E-7)(T_1+273.15)^4 \end{aligned} \tag{6}$$

$$\begin{aligned} C_{p,cu}(T_2) = {} & 342.764033 + (1.33834821E-1)(T_2+273.15) + (5.53525209E-5)(T_2+273.15)^2 \\ & -(1.97122089E-7)(T_2+273.15)^3 + (1.1407471E-10)(T_2+273.15)^4 \end{aligned} \tag{7}$$

herein, k_{cu}, ρ_{cu} and $C_{p,cu}$ are the thermal conductivity, density and specific heat capacity of Cu, respectively.

As the CNTs is selected as filler material of TSVs, the corresponding relationship between temperature and thermophysical properties can be illustrated as (0 ℃ $\ll T \ll$ 100 ℃) [40],

$$k_{CNTs}(T) = 637.931556 + 4.1827T - (1.916922E-3)T^2 - (7.022449E-5)T^3 \tag{8}$$

$$C_{p,CNTs}(T) = 815.37142 + 2.0031428T - (1.2857E-3)T^2 \tag{9}$$

$$\alpha_{CNTs}(T) = 4.4623074E-4 + (7.85775E-8)T + (2.0125771E-8)T^2 - (1.92435E-10)T^3 \tag{10}$$

where, k_{CNTs}, $C_{p,CNTs}$ and α_{CNTs} represent the thermal conductivity, specific heat capacity and thermal diffusivity of CNTs, respectively. The function relationship between the density of CNTs (ρ_{CNTs}) and temperature can be calculated as follows [41],

$$\rho_{CNTs}(T) = \frac{k_{CNTs}(T)}{\alpha_{CNTs}(T)C_{p,CNTs}(T)} \tag{11}$$

When the water is chosen as coolant of micro-channels, the analytical expressions concerning temperature and thermophysical properties of water can be defined as below (0 ℃ ≪ T ≪ 100 ℃) [42],

$$k_{wt}(T) = 0.56112 + (1.93E-3)T - (2.60152749E-6)T^2 - (6.08803E-8)T^3 \tag{12}$$

$$\rho_{wt}(T) = 1000\left[1 - \frac{(T-4)^2}{119000 + 1365T - 4T^2}\right] \tag{13}$$

$$\begin{aligned} C_{p,wt}(T) = {} & 4217.629 - 3.20888T + (9.503E-2)T^2 - (1.32E-3)T^3 \\ & + (9.415E-6)T^4 - (2.5479E-8)T^5 \end{aligned} \tag{14}$$

where, k_{wt}, ρ_{wt} and $C_{p,wt}$ represent the thermal conductivity, density and specific heat capacity of pure water, respectively.

For the CNTs nanofluid as coolant of micro-channels, the relationship between temperature and thermophysical properties of CNTs nanofluid can be defined as [43–45],

$$k_{wt-CNTs}(T) = \frac{1 - \phi + \left(\frac{4\phi}{\pi}\right)\sqrt{\frac{k_{CNTs}(T)}{k_{wt}(T)}}\,\mathrm{arctg}\left(\frac{\pi}{4}\sqrt{\frac{k_{CNTs}(T)}{k_{wt}(T)}}\right)}{1 - \phi + \left(\frac{4\phi}{\pi}\right)\sqrt{\frac{k_{wt}(T)}{k_{CNTs}(T)}}\,\mathrm{arctg}\left(\frac{\pi}{4}\sqrt{\frac{k_{CNTs}(T)}{k_{wt}(T)}}\right)} k_{wt}(T) \tag{15}$$

$$\rho_{wt-CNTs}(T) = \phi\rho_{CNTs}(T) + (1-\phi)\rho_{wt}(T) \tag{16}$$

$$C_{p,wt-CNTs}(T) = \phi C_{p,CNTs}(T) + (1-\phi)C_{p,wt}(T) \tag{17}$$

here, ϕ is the volume fraction of CNTs, $k_{wt-CNTs}$, $\rho_{wt-CNTs}$ and $C_{p,wt-CNTs}$ are the thermal conductivity, density and specific heat capacity of CNTs nanofluid, respectively.

3. Results and discussions

This section will investigate the heat transfer performance of our proposed heat dissipation structure of 3D-ICs (i.e., 3D-ICs with embedded both TSVs and micro-channels), where a five-layers stacked chip is investigated. In order to prove the performance advantage of our proposed heat dissipation structure, we defined the four cases as below, case 1: the 3D-ICs without embedded heat dissipation structure. case 2: the 3D-ICs with only inserted TSVs, case 3: the 3D-ICs with only embedded micro-channels, case 4: the 3D-ICs with embedded both TSVs and micro-channels (i.e., our proposed heat dissipation structure of 3D-ICs). In this work, the inlet temperature of coolant and ambient temperature are set as 20 ℃ and 26 ℃, respectively [46]. Additionally, it is defined that all die layers are configured the same physical geometry structure. The amount of heat generation of per BEOL layer

is set as 2E10 W/m^3, and other physical parameters of 3D-ICs are shown in Table 1 [47–53]. All the calculation results presented in the following section are executed by using the COMSOL 6.0 software. The details of modeling approach for COMSOL simulation are listed as follows [54]:

(1) The heat transfer in solid module is applied in case 1 and case 2 for COMSOL simulation. While the heat transfer in solid and fluid heat transfer module are coupled by using the non-isothermal flow feature in COMSOL simulation for case 3 and case 4.

(2) The total amount of heat generated by heat source is fixed, which is uniformly distributed on each BEOL.

(3) The coolant flow is assumed to be steady, laminar and fully developed in each micro-channel.

(4) The pressure outlet boundary condition of micro-channel is adopted as zero gradients.

(5) The surfaces of micro-channel walls are not affected by slip conditions.

Table 1. The physical and geometric parameters of 3D-ICs.

Parameters	Values
Chip size and square analysis unit size	2000 μm × 2000 μm, 250 μm × 250 μm
Thickness of insulating layer and distance of center to center of TSVs	0.5 μm, 125 μm
Width and height of micro-channels	100 μm, 50 μm
Thickness of package, BEOL, silicon substrate, bonding layer, TIM and heat sink	150 μm, 10 μm, 60 μm, 5 μm, 20 μm, 200 μm,
Density, specific heat capacity and thermal conductivity of package	6240 kg/m^3, 421 J/kg·K, 226 W/m·K
Density, specific heat capacity and thermal conductivity of BEOL	2200 kg/m^3, 517 J/kg·K, 2.25 W/m·K
Density, specific heat capacity and thermal conductivity of silicon substrate	2328.3 kg/m^3, 700 J/kg·K, 150 W/m·K
Density, specific heat capacity and thermal conductivity of bonding layer	1400 kg/m^3, 1100 J/kg·K, 0.3 W/m·K
Density, specific heat capacity and thermal conductivity of TIM	2077 kg/m^3, 870 J/kg·K, 14.416 W/m·K
Density, specific heat capacity and thermal conductivity of heat sink	2688.9 kg/m^3, 902 J/kg·K, 237 W/m·K
Density, specific heat capacity and thermal conductivity of insulating layer	2200 kg/m^3, 765 J/kg·K, 1.4 W/m·K

3.1. Heat transfer performance of 3D-ICs with embedded novel heat dissipation structure

In order to validate the performance superiority of our proposed heat dissipation structure of 3D-ICs, the temperature results of steady-state and transient responses under the defined four cases are investigated, respectively. The transient temperature results for the defined four cases are exhibited in Figure 3. Here, the TSVs radius and the flow rate of coolant are set as 4 μm and 4 mL/min, respectively.

As shown in Figure 3, it is obviously that the swing of temperature fluctuation for the case 1 is larger than all other cases. The reason for this phenomenon is that the heat generation in per BEOL layer cannot be timely transferred to the external environment of 3D-ICs for the case 1. In addition, the characteristics of steady-state response of the defined four cases are investigated, the corresponding steady-state temperature results of all die stacked layer are listed in Table 2.

As displayed in Table 2, it is implied that our proposed heat dissipation structure (i.e., case 4) can remarkably reduce the steady-state temperature of all stacked layer in comparison to case 1, case 2 and case 3. Taking the $i = 5$ die layer as an example, the steady-state temperature for case 4 is reduced over 43.546%, 18.440% and 12.338% respectively, as compared with case 1, case 2 and case 3. Therefore, our proposed heat dissipation structure with embedded both TSVs and micro-channels can effectively improve heat transfer performance of 3D-ICs.

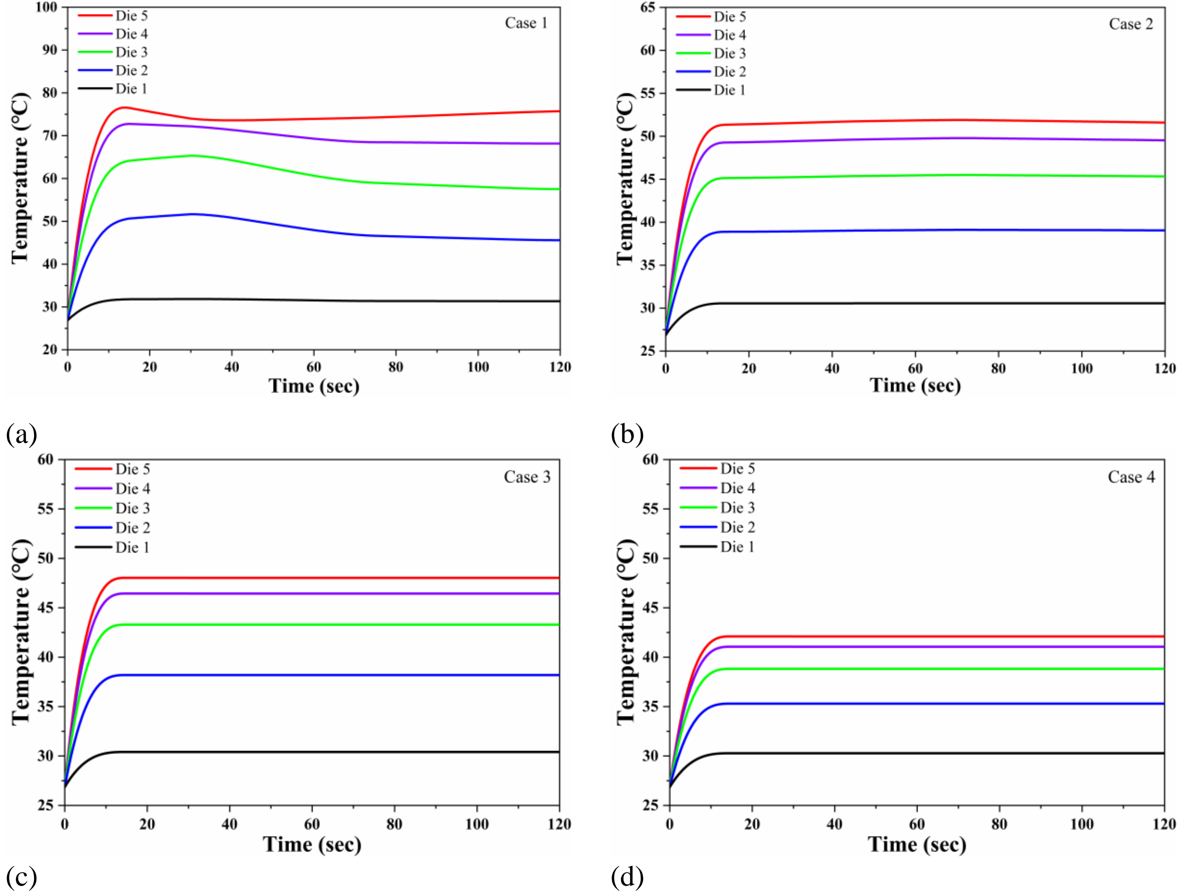


Figure 3. The transient temperature results of per die layer: (a) the 3D-ICs without embedded heat dissipation structure case (i.e., case 1), (b) the 3D-ICs with only inserted TSVs case (i.e., case 2), (c) the 3D-ICs with only embedded micro-channels case (i.e., case 3), (d) the 3D-ICs with embedded both TSVs and micro-channels case (i.e., case 4).

Table 2. The steady-state temperature of all die layer for the defined four cases.

Method	TSVs radius	Flow rate of coolant	Steady-state temperature of ith die layer (°C)				
			$i = 1$	$i = 2$	$i = 3$	$i = 4$	$i = 5$
Case 1	-	-	31.590	48.788	61.685	70.279	74.570
Case 2	4 μm	-	30.560	39.005	45.317	49.531	51.616
Case 3	-	4 mL/min	30.409	38.192	43.292	46.438	48.023
Case 4	4 μm	4 mL/min	30.277	35.298	38.820	41.056	42.098

3.2. Application of CNTs in enhancing heat transfer performance of 3D-ICs

The CNTs as the filler material of TSVs and nanoparticles of nanofluid of micro-channels are investigated in this section respectively, which are adopted as the solutions for enhancing heat transfer

performance of 3D-ICs. In addition, the effects of TSVs radius and flow rate of coolant on the steady-state temperature results of all die layer of 3D-ICs are also analyzed, respectively.

3.2.1 The heat transfer performance of 3D-ICs concerning CNTs for substituting the conventional Cu as filler material of TSVs

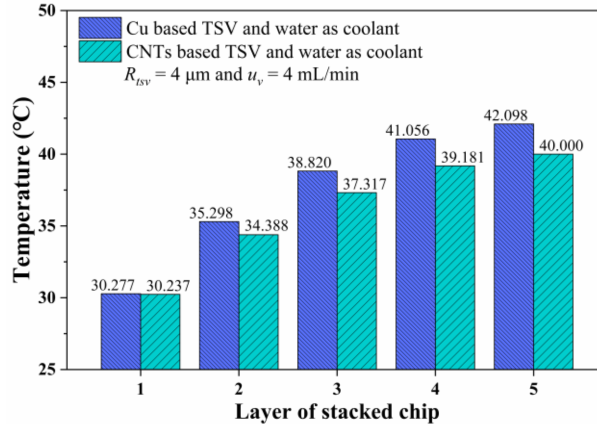


Figure 4. The steady-state temperature results of all die layer under the defined case 4 for using the Cu and CNTs as filler materials of TSVs.

The CNTs as a promising candidate for replacing the traditional Cu as filler material of TSVs are studied to improve heat transfer performance of 3D-ICs in this work. Here, only the defined case 4 for utilizing CNTs and Cu as filler material of TSVs are investigated, the corresponding steady-state results are shown in Figure 4.

As exhibited in Figure 4, it can be observed that the steady-state temperature for CNTs based TSVs case is lower than Cu based TSVs case. Giving the $i = 4$ die layer as an instance, the temperature for CNTs based TSVs case is reduced over 4.567% than the conventional Cu based TSVs case. In addition, the effects of TSVs radius on temperature of all die layer are studied, and the corresponding results are illustrated in Table 3.

As described in Table 3, it is indicated that increasing the TSVs radius can effectively reduce steady-state temperature of all die layer. For instance, when the TSVs radius R_{tsv} increases from 2 μm to 6 μm, the percentage reduction of steady-state temperature is 15.035% at the $i = 4$ die layer. Therefore, increasing the TSVs radius is an effective way to reduce the temperature of 3D-ICs. Moreover, it should be pointed out that the increase of TSVs radius will reduce the layout space of transistor devices and interconnect wires in 3D-ICs.

Table 3. The steady-state temperature of all die layer for CNTs based TSVs with different TSVs radius.

Method	TSVs radius	Flow rate of coolant	Steady-state temperature of ith die layer (°C)				
			$i = 1$	$i = 2$	$i = 3$	$i = 4$	$i = 5$
CNTs based TSVs and water as coolant	2 μm	4 mL/min	30.310	36.408	40.549	43.160	44.411
	3 μm	4 mL/min	30.265	35.322	38.819	41.051	42.008
	4 μm	4 mL/min	30.237	34.388	37.317	39.181	40.000
	5 μm	4 mL/min	30.192	33.696	36.178	37.794	38.405
	6 μm	4 mL/min	30.150	33.152	35.279	36.671	37.155

3.2.2 The heat transfer performance of 3D-ICs concerning CNTs nanofluid for substituting the conventional water as coolant of micro-channels

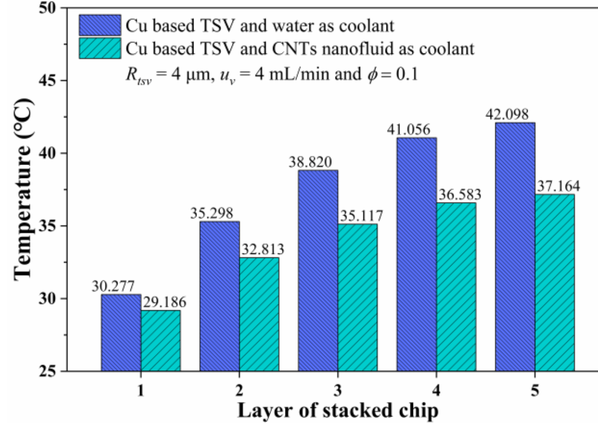


Figure 5. The steady-state temperature results of all die layer for the defined case 4 under the water and CNTs nanofluid as the coolants of micro-channels.

In this section, the CNTs nanofluid for replacing the conventional water as the coolant of micro-channels for promoting heat transfer performance of 3D-ICs is discussed. Herein, only the defined case 4 for water and CNTs nanofluid as coolants are investigated respectively, and corresponding steady-state temperature results are shown in Figure 5. In addition, the filler material of TSVs is adopted as Cu for the defined case 4, meanwhile the volume fraction of CNTs nanoparticles of nanofluid is configured as 0.1.

As depicted in Figure 5, it can be seen that the CNTs nanofluid as coolant case has lower steady-state temperature than the conventional water as coolant scheme. Using the $i = 3$ die layer as an example, the temperature of water as coolant scheme is larger than 1.105 times than CNTs nanofluid as coolant case. The reason behind this is that CNTs nanofluid has a lesser thermal conductivity as compared with water.

Table 4. The steady-state temperature of all die layer for CNTs nanofluid as coolant with different flow rate of coolant.

Method	TSVs radius	Flow rate of coolant	Steady-state temperature of ith die layer (°C)				
			$i = 1$	$i = 2$	$i = 3$	$i = 4$	$i = 5$
Cu based TSVs and CNTs nanofluid as coolant	4 μm	2 mL/min	29.977	35.412	39.129	41.540	42.548
	4 μm	3 mL/min	29.520	33.901	36.787	38.638	39.389
	4 μm	4 mL/min	29.186	32.813	35.117	36.583	37.164
	4 μm	5 mL/min	28.927	31.988	33.865	35.052	35.513
	4 μm	6 mL/min	28.720	31.337	32.890	33.868	34.244

Additionally, the impacts of coolant flow rate of micro-channels on steady-state temperature of all die layer are shown in Table 4, where the coolant of micro-channels is selected as CNTs nanofluid. Table 4 indicates that increasing the flow rate of coolant can significantly reduce the steady-state temperature of all die layer of 3D-ICs. For instance, the steady-state temperature can be reduced over 15.945% when the flow rate of coolant u_v increases from 2 mL/min to 6 mL/min at the $i = 3$ die layer. Therefore, increasing the flow rate of coolant can evidently enhance heat transfer performance of 3D-

ICs. In addition, it ought to be stated that the increase in flow rate of coolant is due to the increase of pump power.

3.2.3 The heat transfer performance of 3D-ICs with embedded both CNTs as filler material of TSVs and CNTs nanofluid as coolant of micro-channels

On the basis of the aforementioned discussions, the heat transfer performance of 3D-ICs with embedded both CNTs as filler material of TSVs and CNTs nanofluid as coolant of micro-channels are investigated in this section. The corresponding steady-state temperature results for the defined case 4 are depicted in Figure 6. Here, in order to analyze conveniently, we defined the four schemes as follows, Scheme 1: the filler material of TSVs is adopted as the conventional Cu, and the coolant of micro-channels is configured as the conventional water. Scheme 2: the filler material of TSVs is adopted as the CNTs, and the coolant of micro-channels is also configured as the conventional water. Scheme 3: the filler material of TSVs is also adopted as the conventional Cu, and the coolant of micro-channels is configured as the CNTs nanofluid. Scheme 4: the filler material of TSVs is adopted as the CNTs, and the coolant of micro-channels is configured as the CNTs nanofluid.

Figure 6 shows that the proposed scheme 4 has lower steady-state temperature than all other schemes (i.e., scheme 1, scheme 2 and scheme 3). As an instance, for the $i = 4$ die layer, the steady-state temperature of scheme 4 is reduced by 13.767%, 10.895% and 4.567% in comparison to scheme 1, scheme 2 and scheme 3 respectively. Consequently, the proposed scheme 4 (i.e., 3D-ICs with embedded both CNTs as filler material of TSVs and CNTs nanofluid as coolant of micro-channels) can be regarded as a prospective approach for enhancing heat transfer performance of 3D-ICs.

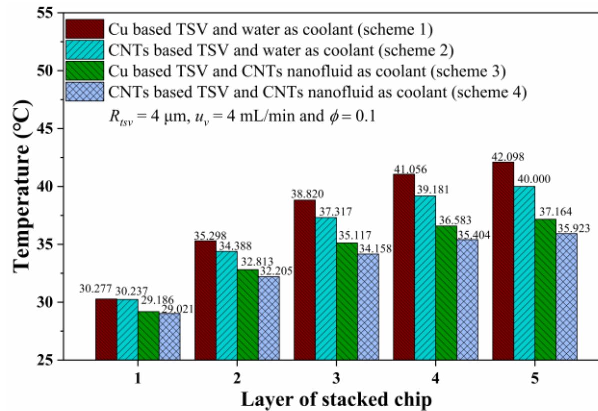


Figure 6. The steady-state temperature results of all die layer for the defined case 4 under the defined four schemes.

Besides, the influences of TSVs radius and flow rate of coolant on the steady-state temperature of 3D-ICs are studied. And the corresponding steady-state temperature results with different TSVs radius and flow rate of coolant are listed in Table 5. Here, only the proposed scheme 4 is investigated.

As illustrated in Table 5, it is suggested that increasing both TSVs radius and flow rate of coolant can further enhance heat transfer performance of 3D-ICs. Taking the $i = 3$ die layer as an example, the steady-state temperature for R_{tsv} = 2 μm and u_v =2 mL/min case is 1.271 times larger than R_{tsv} = 6 μm and u_v =6 mL/min case. Therefore, increasing the TSVs radius and flow rate of coolant of micro-channels can greatly improve heat transfer performance of 3D-ICs.

Table 5. The steady-state temperature results of all die layer for different TSVs radius and flow rate of coolant.

Method	TSVs radius	Flow rate of coolant	Steady-state temperature of ith die layer (°C)				
			$i = 1$	$i = 2$	$i = 3$	$i = 4$	$i = 5$
Scheme 4	2 μm	2 mL/min	30.076	36.161	40.293	42.899	44.130
	3 μm	3 mL/min	29.484	33.695	36.442	38.173	38.897
	4 μm	4 mL/min	29.021	32.205	34.158	35.404	35.923
	5 μm	5 mL/min	28.793	31.247	32.702	33.638	33.965
	6 μm	6 mL/min	28.625	30.576	31.696	32.426	32.649

4. Conclusions

A new heat dissipation structure concerning 3D-ICs with embedded both TSVs and micro-channels (i.e., the proposed case 4) is proposed to enhance heat transfer performance of 3D-ICs in this paper. The COMSOL simulation model for the defined four cases is established to analyze heat transfer performance of steady-state and transient responses respectively, which take the effects of temperature on filler material of TSVs and coolant of micro-channels into consideration in this work. The main findings of this work are listed as follows:

(1) Our proposed heat dissipation structure (i.e., the proposed case 4) can remarkably enhance heat transfer performance of 3D-ICs. The steady-state temperature for case 4 is reduced over 43.546%, 18.440% and 12.338% respectively, as compared with the defined case 1, case 2 and case 3.

(2) The proposed scheme 4 can be regarded as a prospective approach for improving heat transfer performance of 3D-ICs. For the proposed case 4, the steady-state temperature of scheme 4 can be reduced by 13.767%, 10.895% and 4.567% as compared with the defined scheme 1, scheme 2 and scheme 3, respectively.

(3) The heat transfer performance of 3D-ICs with integrated the proposed heat dissipation structure can be further improved by the increase of TSVs radius and flow rate of coolant of micro-channels.

Based on the presented results in this paper, our proposed new heat dissipation structure would be beneficial in enhancing heat transfer performance to solve the complex heat problems of 3D-ICs. However, it must be emphasized that the preparation of 3D-ICs with integrated the proposed heat dissipation structure requires the sophisticated equipment, meanwhile have also the high requirement in the complex fabrication procedures. Therefore, the fabrication of 3D-ICs with integrated the proposed heat dissipation structure might be the biggest challenge in the practical application.

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