AN EQUIVALENT THERMAL CONDUCTIVITY MODEL OF TSV ARRAYS FOR THERMAL ANALYSIS IN 3-D INTEGRATED CIRCUITS

by

Zhao-Pei XU [a], ***Kang-Jia WANG*** [a,*]

[a] School of Physics and Electronic Information Engineering,
Henan Polytechnic University, Jiaozuo, China.

As the CMOS technology continuously scales down into the deep submicron regime and approaches the physical limits of minimization, Moore's Law is hindered. The proposed three-dimensional integrated circuit (3-D IC) technology based on through silicon via (TSVs) brings hope. Although 3-D ICs bring many advantages over 2-D ICs, the thermal management challenges still need to be addressed effectively. TSVs carry signals while facilitating the thermal transfer of stacked chips due to their high thermal conductivity and offer a potential thermal management solution for 3-D ICs. The TSVs are structured in arrays to significantly improve heat dissipation. This paper proposes a cellular array structure that offers better heat dissipation capabilities compared to conventional rectangular arrays. First, the TSV cellular arrangement is described. Secondly, a method for modelling the equivalent thermal conductivity (ETC) of TSV arrays is proposed. Finally, the excellent performance of the cellular structure on thermal conductivity is verified by a comparative analysis of the thermal characteristics of the TSV array in the COMSOL system using finite element method(FEM). The results presented in this paper are beneficial for designers to optimise the TSV array arrangement and predict the thermal performance of TSV arrays. In addition, it provides a reference for 3-D IC reliability design.

Keywords*: 3-D IC, ETC, thermal analysis, FEM.*

1. Introduction

Recently, with the development of microelectronic technology, integrated chips are developing towards miniaturization and multi-integration[1,2]. To solve the demand for the development and innovation of integrated circuits, 3-D integrated circuits(3-D ICs) based on TSV vertical interconnection technology came into being[3]. 3-D ICs have several advantages such as small wirelength, low power consumption and high bandwidth[4,5]. The characteristic size of chips decreases year by year, which leads to the number of integrated semiconductors per unit area and the power of electronic components in unit volume increasing gradually. How to reduce temperature becomes the first priority faced by 3-D ICs. Especially, local high temperature region caused by hotspots brings great challenges to the performance of electronic products[6,7].

* Corresponding author; e-mail:konka05@163.com

The TSV array structure has attracted a significant interest from academics because of its ability to significantly improve heat dissipation.

Various approaches have been proposed to address thermal issues in 3-D ICs [8,9]. The structure of the TSV includes cylindrical [10], conical [11], coaxial [12] and tapered [13]. The influence of structural parameters such as the inclination angle of the conical ring TSV and the thickness of the insulation layer on the heat transfer characteristics are investigated[14]. In [15], the influence of height, diameter and shape of TSVs are analyzed on the heat dissipation. In[16], the heat transfer performance of TSV was analysed for different filling materials. An equivalent thermal model of 3-D IC based on the MLGNR structure is proposed, which takes into account the lateral heat transfer TSVs[17]. The effects of 3-D IC with different TSV models and different material-filled, AR and dielectric thermal conductivity on the steady-state temperature profiles are studied[18].

It is notable that the majority of aforementioned works describe a single TSV. The TSVs in 3-D ICs generally exist in an array form, as shown in Fig. 1, which means thermal results caused by TSV arrays may be dramatically different from those caused by a single TSV. A general approach has been proposed for predicting the temperature and thermal stress fields of TSV arrays in 3-D IC based on a coupled-field finite-element (FE) method[19]. The method is proposed to eliminate dynamic hotspots in 3-D IC by using switching signals in TSV clusters.[20]. A square triangular TSV array structure is proposed and shown to be an efficient way to alleviate the thermal problems in 3-D ICs[21]. In[22], it demonstrates a TSV integrated thermoelectric cooling that provides exceptional hot spot cooling performance combined with passive cooling from a metal TSV and active cooling from multi-porous silicon.

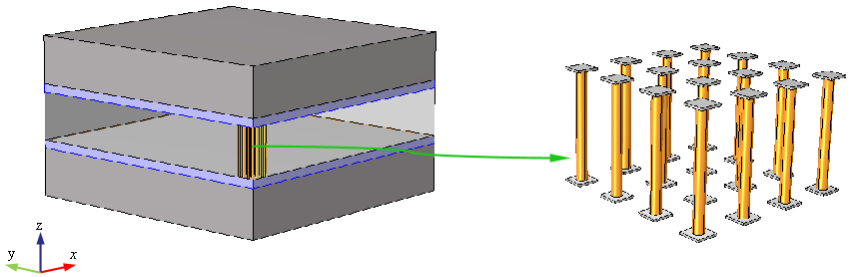

Figure 1. TSV array structure diagram of 3-D IC.

To sum up, for the thermal research of tsv and 3D integrated circuits, thermal simulation analysis is mainly carried out for a single tsv. The main innovation of this paper is to establish the ETC model of TSV arrays of various structures, which can be used to calculate the ETC of TSV arrays of various structures and arrangements. The factors affecting the thermal transmission performance of TSV network are analyzed, and the configuration of TSV network is optimized. The thermal characteristics of TSV array in COMSOL system are compared and analyzed by finite element method, and the excellent thermal conductivity of honeycomb array structure is verified, which has certain guiding value for the research of 3D integrated circuit.

The rest of this paper is organized as follows: The methodology of ETC of TSV arrays is proposed in Section 2. Simulation results and analysis of ETC are presented in Section 3. The whole article is concluded in Section 4.

2. Methodology of ETC

In this section, We deduce an equation for the ETC of the TSV array and verified its accuracy in COMSOL. The thermal conductivity of the TSV array is obtained by assimilating it to a model having the

same dimensions and thermal conductivity as the real array. TSV-filled materials have high thermal conductivity. The thermal conductivity of the TSV array is anisotropic and needs to be calculated separately.

2.1 ETC in the vertical direction

In order to minimise the error between the ETC calculations and reality, the modelling needs to take into account as many details of the overall TSV structure as possible. The TSV array can be divided into a set of a finite number of identical basic units. Therefore, a single TSV can be extracted as the basic unit for computation. The basic unit is equivalent to a simple model with the same dimensions, but with a unique overall heat conductivity. Fig. 2 presents the physical structure of the TSV basic unit. The entire basic unit is divided into five sections, A1/A2: the pad section, both of which have a height of t_1; B1/B2: the upper and lower isolation layer sections, both of which have a height of t_2; and C: the main TSV section, which has a height of t_3. These five components are connected in series to form a heat conduction path in the vertical direction. The radius of the solder disc is r_1, the radius of the TSV is r_2 and the thickness of the insulation layer is r_3. t is the height of the whole model, i.e. $t = 2t_1 + 2t_2 + t_3$.

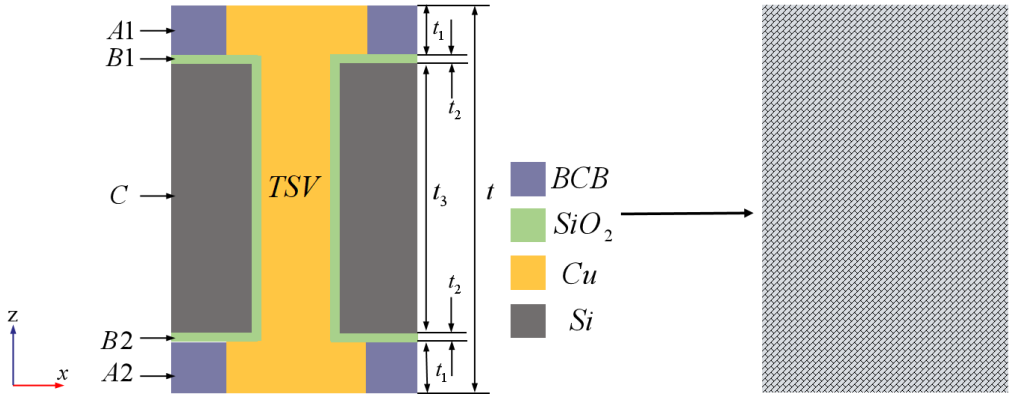

Figure 2. Physical structure of the TSV basic unit.

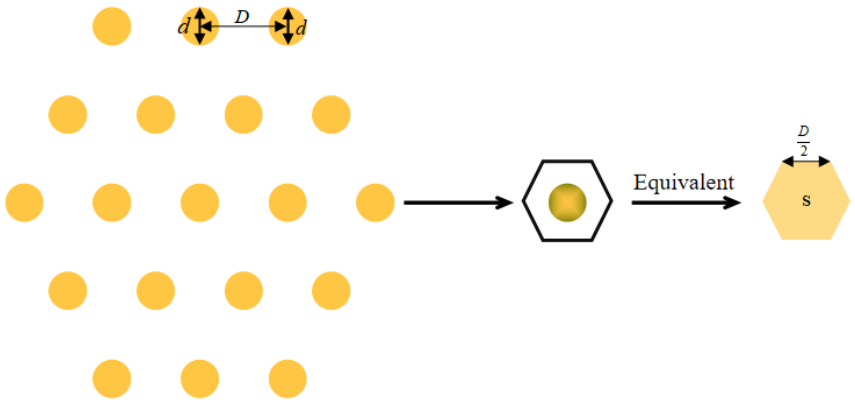

Figure 3. ETC of cellular TSV array

Using the parallel thermal resistance calculation method, the K_A of part A1/A2 can be derived as:

$$K_A = K_{Cu} \cdot \alpha + K_{BCB} \cdot (1-\alpha). \quad (1)$$

$$\alpha = \frac{\pi r_1^2}{s}. \quad (2)$$

Where K_{Cu} and K_{BCB} are the thermal conductivity of the Cu and BCB materials respectively. α is

the overall area ratio occupied by the TSV pads. s is the area of the entire calculation cell in the lateral plane.

For part B1/B2, the equivalent thermal conductivity K_B can be given by:

$$K_B = K_{Cu} \cdot \beta + K_{SiO_2} \cdot (1-\beta). \tag{3}$$

$$\beta = \frac{\pi r_2^2}{s}. \tag{4}$$

Where K_{SiO2} is the thermal conductivity of SiO_2. β is the global area ratio occupied by the cross section of the TSV tube core. For part C, the equivalent thermal conductivity K_C can be obtained:

$$K_C = K_{Cu} \cdot \beta + K_{SiO_2} \cdot \gamma + K_{Si} \cdot (1-\beta-\gamma). \tag{5}$$

$$\gamma = \frac{\pi (r_2 + r_3)^2 - \pi r_3^2}{s}. \tag{6}$$

Where K_{Si} is the thermal conductivity of Si. γ is the ratio of the overall occupied by the cross section of the insulation layer.

Therefore, the ETC of the basic unit $K_{zTSVunit}$ can be expressed:

$$K_{zTSVunit} = \frac{t}{\frac{2t_1}{K_{Cu} \cdot \alpha + K_{BCB} \cdot (1-\alpha)} + \frac{2t_2}{K_{Cu} \cdot \beta + K_{SiO_2} \cdot (1-\beta)} + \frac{t_3}{K_{Cu} \cdot \beta + K_{SiO_2} \cdot \gamma + K_{Si} \cdot (1-\beta-\gamma)}}. \tag{7}$$

2.2 ETC in the lateral direction

The lateral thermal conductivity of the TSV has a significant effect on the temperature distribution of the 3-D IC [23]. Considering detailed geometries results in increased model complexity and computational costs. When heat is transferred laterally from the TSV elementary unit, the heat flow is perpendicular to the SiO_2 insulation layer and the thermal resistance can be expressed as:

$$R_{\text{bound}} = \int_{r_2}^{r_2+r_3} \frac{dr}{2\pi r t k_{ins}}. \tag{8}$$

The impact of the SiO_2 insulation layer filled between Cu and Si is simplified to the thermal boundary resistance. Its thermal conductivity can be expressed as:

$$h_{ins} = \frac{1}{2\pi r_2 t R_{bound}}. \tag{9}$$

$K_{xyTSVunit}$ can be represented as:

$$K_{xyTSVunit} = K_{Si} \frac{\left(\frac{K_{Cu}}{K_{Si}} - \frac{K_{Cu}}{h_{ins} r_2} - 1\right)\eta + \frac{K_{Cu}}{h_{ins} r_2} + \frac{K_{Cu}}{K_{Si}} + 1}{\left(-\frac{K_{Cu}}{K_{Si}} + \frac{K_{Cu}}{h_{ins} r_2} + 1\right)\eta + \frac{K_{Cu}}{h_{ins} r_2} + \frac{K_{Cu}}{K_{Si}} + 1}. \tag{10}$$

Here, η is the volume fraction of the base cell occupied by the TSV. The above derivative formulae are applicable to various TSV array structures. Only the relevant values of α, β, γ and η are modified. The final equivalent result is shown in Fig. 3.

3. Results and discussion

In this section, We explain the method for obtaining the effective thermal conductivity through COMSOL. A good fit between the analytical solution and the FEM simulation is obtained by verification. The effects of different TSV spacings, TSV diameters, and thermal conductivities of the insulation on the equivalent thermal conductivity are compared.

3.1 Simulation validation of ETC of TSV basic units

Finite element methods have been applied to calculate the ETC of complex structures. For non-homogeneous materials, ETC can be obtained by COMSOL simulation. The specific steps are as follows:

Create a heat transfer model in COMSOL, including the geometry and thermal boundary conditions of the non-uniform material. The TSV layout is a cellular structure. The thermal conductivity distribution of a non-homogeneous material is defined in the model, which can be described using functions or tables. The relevant parameters of the TSV basic unit are as follows: t = 100 um, K_{Cu} = 400 Wm-1K-1, K_{Si} = 148 Wm-1K-1, K_{BCB} = 0.3 Wm-1K-1, K_{SiO2} = 30 Wm-1K-1, r_2 = D/2 , r_1 = r_2+2. TSV spacing is 20 um. Insulation layer thickness r_3 is 0.1 um, its thermal conductivity is set to 30 Wm-1K-1. t_1 is set to 5 um. t_2 is set to 2 um. Run the model to obtain the temperature distribution of the non-uniform material. ETC is calculated from the temperature distribution, using the average value function in COMSOL. The accuracy of the ETC is verified by comparison with experimental data or theoretical calculations. The analytical and simulation solutions are obtained using the above equations and FEM.

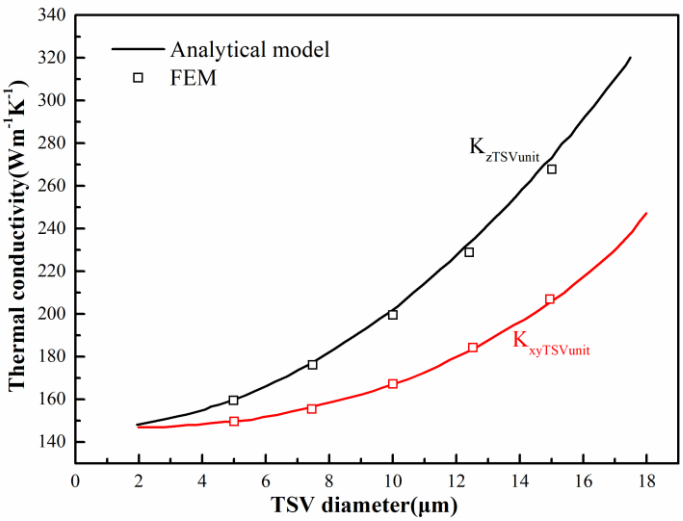

Figure 4. Effective lateral and vertical thermal conductivities of the TSV unit cell with varying dimensions.

From Fig. 4, it can be concluded that there is a good agreement between the analytical solution and FEM of the ETC of the TSV basic unit. The maximum error between the analytical and simulation solutions is 1.98% in the vertical direction and 0.73% in the horizontal direction. The calculation method proposed in this paper has a high degree of accuracy. However, it can also be concluded that the error becomes larger as the TSV diameter increases. The thermal conductivity of the TSV base unit is anisotropic, and therefore the thermal conductivity in all directions cannot be assimilated as a constant.

3.2 ETC analysis of TSV array arrangement structures

The other parameters remain unchanged and the range of D is extended to 7.5 - 25 um, calculating the ETC in each direction for both layouts. As shown in Fig. 4, the ETC in each direction decreases with increasing spacing. Where CS and SS represent cellular and square structures respectively. The dashed and solid lines represent high and low thermal conductivity insulating materials respectively. It is clear from the graph that the ETC of the CS is significantly higher than that of the SS at the same spacing. The results show that increasing the thermal conductivity of the insulation layer is beneficial for chip heat dissipation.

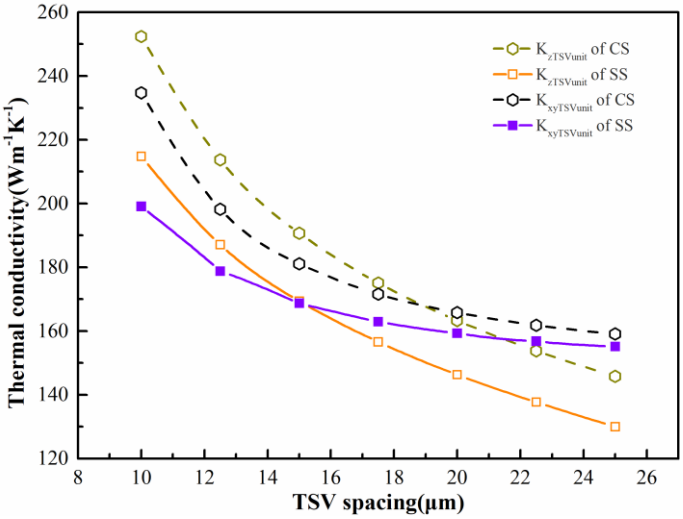

Figure 5. Vertical ETC under different TSV spacings and TSV Layout Structures.

The range of d is extended to 2.5 - 17.5 um in 2.5 um steps. The ETC of the TSV is calculated for the two structures of the arrangement at different diameters. According to Fig. 6(a), the ETC in the vertical direction increases as the TSV diameter increases. As shown in Fig. 6(b), the ETC in the horizontal direction becomes significantly larger as the TSV diameter increasing. ETC is significantly greater in the horizontal direction than in the vertical direction. The solid red and black lines in the diagram represent low thermal conductivity and higher thermal conductivity of the insulation layer respectively.

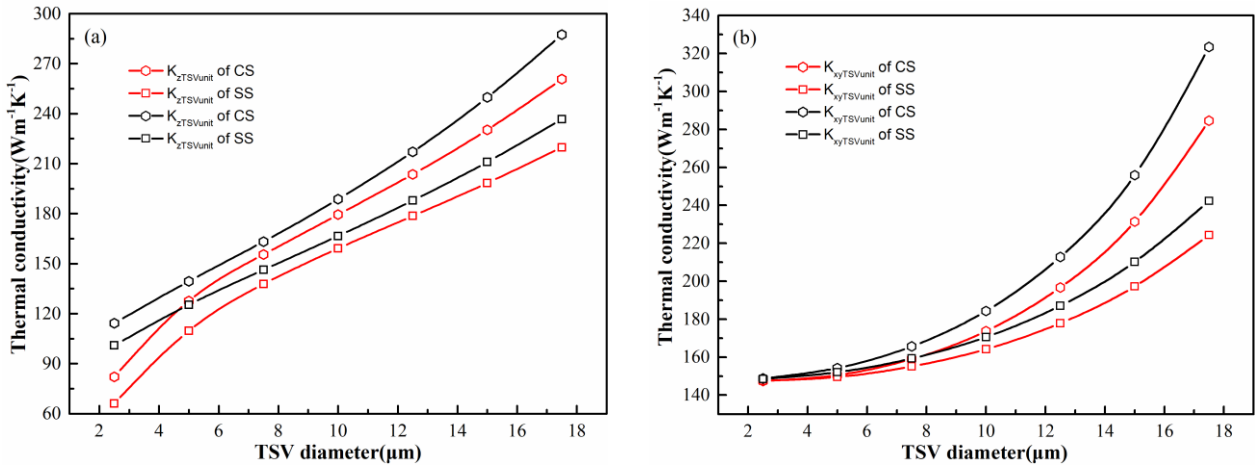

Figure 6. ETC under different TSV diameters and TSV Layout Structures. (a) Vertical ETC; (b) Lateral ETC.

Comparing the two types of layout, the thermal conductivity of the cellular structure is higher than that of the square arrangement for different diameters and TSV spacing. This also indicates that the proposed

structure has higher thermal conductivity in all directions and its thermal performance is better.

4. Conclusion

The analytical solutions fit well with the FEM simulations. The lateral thermal conductivity is much smaller compared to that of the vertical direction. Simply using the vertical thermal conductivity of TSV for both lateral and vertical directions will overestimate its cooling performance in reducing the peak temperature. Besides, the influence of TSV spacing, TSV diameter and insulation material on heat transfer characteristics and ETC are studied. The proposed equivalent thermal conductivity provides a way for the numerical calculation of the temperature of three-dimensional integrated circuits containing TSV. In the future, we can use this method to calculate the chip temperature of more complex structures. The main conclusions are as follows:

(1) We establish the equations to solve for the ETC of the TSV array. Based on the previous comparisons of experimental results, it is shown that the results obtained by the proposed method in the paper have close agreement with FEM. T his method is applicable to a variety of TSV array structures.

(2)The effect of TSV spacing on ETC is investigated and it is found that ETC decreases as the spacing increases. However, the variation rate in the vertical direction is significantly higher than that in the horizontal direction.

(3)In addition, the TSV ETC as the TSV diameter increases, but the change rate is significantly higher in the horizontal direction than in the vertical direction. The discovery of insulating layer materials with high thermal conductivity can facilitate a significant improvement in ETC.

(4)Moreover, the ETC is significantly better in all directions for the CS than SS.

Acknowledgement

This work is supported by the Key Programs of Universities in Henan Province of China (22A140006), the Fundamental Research Funds for the Universities of Henan Province (NSFRF210324), Program of Henan Polytechnic University (B2018-40), Innovative Scientists and Technicians Team of Henan Provincial High Education (21IRTSTHN016).

Nomenclature

R－thermal resistance, [K • W^{-1}]

K－coefficient of thermal conductivity, [W • (m • K)$^{-1}$]

h－thermal conduction, [W • K^{-1}]

t－height of TSV unit, [μm]

r－radius, [μm]

D－TSV spacing, [μm]

d－TSV diameter, [μm]

Greek symbols

α－area occupied by the TSV pads

β－area occupied by the insulator layer of B

γ－area occupied by the insulator layer of C

η－volume fraction of TSV

Subscripts

ins－insulator

BCB－bonding layer

CS－cell

SS－ambient

A－the pad section of TSV unit

B－the isolation layer sections of TSV unit

C－the main TSV section of TSV unit

xyTSVunit －the lateral direction of TSV unit

zTSVunit－the vertical direction of TSV unit

References

[1] Wang, K. J. and Pan, Z. L., An Analytical Model for Steady-State and Transient Temperature Fields in 3-D Integrated Circuits, IEEE Trans. Packag., Manuf. Technol., 6 (2016), 7, pp. 1026-1039

[2] Wang, X., et al., Modifying the thermal conductivity of small molecule organic semiconductor thin films with metal nanoparticles, Sci. Rep. 5 (2015) 16095

[3] Shen, W. W. and Chen, K. N., Three Dimensional Integrated Circuit (3D IC) Key Technology: Through Silicon Via (TSV), Nanoscale Research Letters, 12 (2017), 1, pp. 56-60

[4] Van der Plas G, Limaye P, Loi I, et al., Design Issues and Considerations for Low-cost 3-D TSV IC Technology, IEEE Jourrnal of Solid- State Circuits, 46 (2011), 1, pp. 293-307

[5] Tianming Ni, et al., Architecture of Cobweb-Based Redundant TSV for Clustered Faults, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, 28(2020), 7

[6] D. Ansari, K.-Y. Kim, Hotspot management using a hybrid heat sink with stepped pin-fins, Numer. Heat Tran., Part A: Applications, 75 (2019), pp. 359-380

[7] He, Z., et al., Combustion characteristics and thermal enhancement of premixed hydrogen/air in micro combustor with pin fin arrays, Int. J. Hydrogen Energy 45 (2020), pp. 5014-5027

[8] S. G. Kandlikar, Review and projections of integrated cooling systems for three-dimensional integrated circuits, J. Electron. Packag., 136 (2014), 2, pp. 024001

[9] K. Pietrak and T. S. Wisniewski, A review of models for effective thermal conductivity of composite materials, J. Power Technol., 95 (2015), 1, pp. 14–24

[10] Xie, B., Swaminathan M., FDFD Modeling of Signal Paths With TSVs in Silicon Interposer, IEEE Transactions on Components, Packaging and Manufacturing Technology, (4)2014, 4, pp. 708-717

[11] Lu, T., Srivastava A., Modeling and Layout Optimization for Tapered TSVs, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 23 (2015), 12, pp. 1-1

[12] Zhao, w. s., Wang, X. P., Xu, X. L., et al., Electrothermal modeling of coaxial through silicon via(TSV) for three-dimensional ICs, IEEE Electrical Design of Advanced Package & Systems Symposium, 2010

[13] Xu, X. L., Zhao, W. S., Yin, W. Y., Modeling of a pair of annular through silicon vias (TSV), Electrical Design of Advanced Packaging & Systems Symposium, 2011

[14] Xu, Z. P. and Wang, K. J., An Analytical Thermal Model for the 3-D ICS with New-type Through Silicon Via, Thermal Science, 27 (2023), 3B, pp. X-8

[15] Park, M., et al., Evaluation of Si Liquid Cooling Structure with Micro-channel and TSV for 3D Application, Microsyst Technol, 23 (2017), 5, pp. 2609-2614

[16] Qian, L., Zhu, Z., Analytical heat transfer model for three-dimensional integrated circuits incorporating through silicon via effect-RETRACTED, Micro & Nano Letter, 7 (2012), 9, pp. 994-996

[17] Xu, P., et al., Thermal Model for 3-D Integrated Circuits with Integrated Mlgnr-Based, THERMAL SCIENCE, 24 (2020), 3B, pp. 2067-2075

[18] Wang, K. J., et al., Thermal Management of the Through Silicon Vias in 3-D Integrated Circuits, THERMAL SCIENCE, (23) 2019, 4, pp. 2157-2162

[19] Zhang, C. B., and Li, L. J., Characterization and Design of Through-Silicon Via Arrays in Three-Dimensional ICs Based on Thermomechanical Modeling, IEEE TRANSACTIONS ON ELECTRON DEVICES, 58 (2011), 2

[20] H, L. G., et al., A method to alleviate hot spot problem in 3D IC, Microelectronic Engineering, S0167931718300042. doi:10.1016/j.mee.2018.01.004

[21] Hou L, Fu J, Wang J, et al., A novel thermal-aware structure of TSV cluster in 3D IC, Microelectron. Engin., 2016, 153, pp. 110-116

[22] Ren, Z. Q., et al., TSV integrated thermoelectric cooling by holey silicon for hot spot thermal management, Nanotechnology, 2019

[23] Y. Chen, E. Kursun, D. Motschman, C. Johnson, and Y. Xie, Through silicon via aware design planning for thermally efficient 3-D integrated circuits, IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., 32 (2013), 9, pp. 1335-1346

Submitted: 19.9.2023.
Revised: 01.4.2024.
Accepted: 19.4.2024.