

## THERMAL MODELLING AND ANALYSIS OF 3-D INTEGRATED CIRCUITS WITH IRREGULAR STRUCTURE

by

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*Considering the manufacturing and packaging process, 3-D integrated circuits design often requires irregular chip structures. The 3-D integrated circuits with irregular structures can facilitate differentiated chip design and reduce manufacturing costs. Highly complex through-silicon vias have not been considered in past thermal modelling and analysis of irregularly structured 3-D integrated circuits. Thus, a detailed model of a three-layer irregularly structured 3-D integrated circuit with through-silicon vias and microbumps is developed, and an analytical method based on the thermal resistance network model is proposed to extract the equivalent thermal conductivity of through-silicon vias and microbumps, the accuracy of which is verified by a 3-D finite element simulation method. The results show that the maximum temperature and temperature gradient obtained by the equivalent model simulations agree well with the detailed model results, proving the validity of the equivalent model. To save the computational cost, the effects of heat source area, power setting and through-silicon vias structure parameters on the maximum temperature are studied by numerical simulation method based on the equivalent model. Heat source area equal to the overlap between chip layers, high power chips close to the heat sink, and reducing through-silicon vias pitch can better reduce the maximum temperature. The results provide a reference value for thermal design and optimization of 3-D integrated circuits with irregular structures.*

**Key words:** 3-D integrated circuits, irregular structure, numerical simulation, through-silicon via, equivalent thermal conductivity model, maximum temperature

### Introduction

In recent years, 3-D integrated circuits (IC) have become the mainstream research object in the current semiconductor industry. The 3-D integration with through-silicon vias (TSV) offers the shortest interconnection paths between chips in 3-D IC, which reduces electrical interconnection delays and power consumption. Meanwhile, 3-D heterogeneous integration also enables devices with higher performance, miniaturization, and multi-function [1-3]. However, the high-power density and multilayer nature of 3-D IC also results in more stringent design challenges on thermal management. Hot spots and heat-related issues not only degrade the performance of 3-D IC [4] but also seriously affect their reliability [5, 6]. As a result, we

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must accurately predict temperature distributions of 3-D IC as soon as possible in the early thermal-electrical codesign stage to overcome the thermal management dilemma, which is also helpful for the performance optimization of 3-D IC.

In the early design steps, accurate and rapid assessment of the internal temperature distribution of 3-D IC is especially important. From a thermal perspective, modelling of heat transfer in 3-D IC has been conducted to obtain temperature information based on a variety of techniques, which can be broadly divided into analytical approaches [7-9] and numerical simulation [10, 11], such as the FEM, thermal resistance network model [12-14], finite volume method [15], Green's function [16, 17], and so on. Thermal analysis provides temperature distribution information and data basis for thermal management. The purpose of thermal management is to avoid hot spots and achieve lower thermal gradients through obtaining precise temperature distribution information. Recent research literature has proposed numerous approaches for peak chip temperature analysis and co-optimization, which mainly focus on TSV lay-out optimization [18-21], heat source lay-out optimization [22], and thermal plane lay-out optimization [23].

Considering the manufacturing and packaging process, the design of 3-D IC often requires irregularly structured chips [24], which not only helps to reduce design and manufacturing costs, but also promotes the development of heterogeneous integration [25-27]. The heat transfer paths and heat transfer characteristics of irregularly structured 3-D IC are significantly different from those of regularly structured 3-D IC. Most previous thermal analyses of 3-D IC have been performed for regular structured chips [28-32]. Although few studies have been performed for 3-D IC with irregular structured chips, the details of TSV and microbumps were neglected [33-36], which have important effects on heat transfer characteristics [37, 38]. Therefore, comprehensive studies on the thermal performance of irregularly structured 3-D IC are still needed.

In this paper, a three-layer irregular 3-D IC model containing TSV and microbumps is developed, and an analytical method based on the thermal resistance network model is proposed to derive the in-plane and out-of-plane equivalent thermal conductivity for TSV and microbumps. In addition, the effects of various parameters on the thermal behavior of 3-D IC with irregular structures, such as heat source area, total power, power distribution and TSV structure parameters, are investigated by numerical simulations based on equivalent model of irregular structures. Our research work facilitates the thermal design and optimization of 3-D IC with irregular structures.

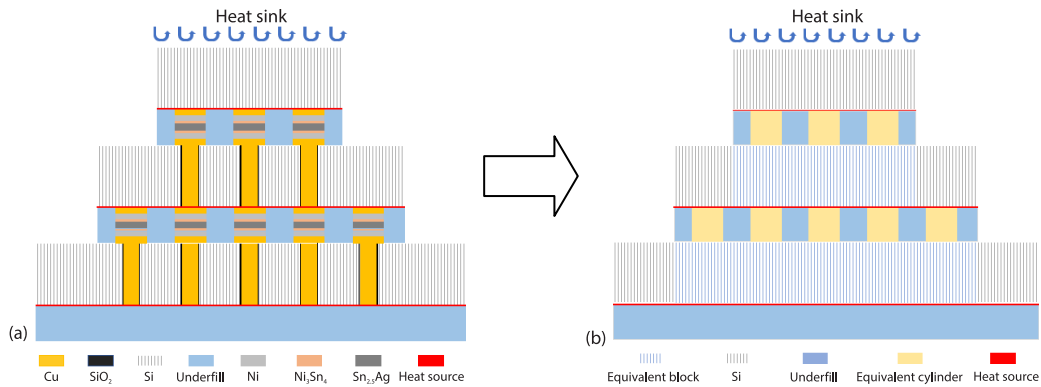
### **Compact model and analysis methods**

To study the heat transfer characteristics of irregularly structured 3-D IC, a typical three-layer 3-D IC model with irregular structure is proposed in this study. Due to the high computational cost of the detailed 3-D IC model, it is necessary to simplify the FEM model, primarily the TSV and micro-bumps with cross-scale structures and a range of composite materials. The equivalent model is introduced to evaluate the heat transfer performance of irregularly structured 3-D IC. The numerical simulations are performed by COMSOL 5.5 software.

#### *Physical model*

Figure 1 depicts a three-layer 3-D IC model with irregular structure, based on 3D IC model obtained from relevant literatures [10, 11, 13, 33]. Figures 1(a) and 1(b) show the cross-sectional views of the detailed and equivalent 3-D IC models cut along the mid-vertical line, respectively. As shown fig. 1(b), the detailed TSV and micro-bumps are replaced by

equivalent anisotropic thermal conductivity blocks in the equivalent model, respectively. The structural parameters in the detailed 3-D IC model are listed in tab. 1 based on the relevant literature [10, 39, 40].



**Figure 1. Cross-sectional view of irregularly structured 3-D IC; (a) detailed model and (b) equivalent model**

**Table 1. Parameters of each structure in the detailed model**

Structure	Value [ $\mu\text{m}$ ]
First layer chip (from bottom to top)	$280 \times 280 \times 50$
Second layer chip	$200 \times 200 \times 50$
Third layer chip	$120 \times 120 \times 50$
Diameter of Cu in TSV	16
Diameter of TSV containing SiO <sub>2</sub> layer	18
Height of micro bumps	23
Diameter of micro bumps	20
Thickness of Ni	3
Thickness of Ni <sub>3</sub> Sn <sub>4</sub>	1.5
Thickness of Sn <sub>2.5</sub> Ag	4
Thickness of Cu in the micro-bump	5

*Control equation and boundary conditions*

The simulation is based on a steady-state heat transfer analysis, where the heat flow in 3-D IC is in a controlled area of a solid with isotropic and anisotropic thermal conductivity:

$$\rho C_p \frac{\partial T}{\partial t} - \nabla(k \nabla T) = Q \tag{1}$$

where  $Q$  is the heat flow.

In order to exclude the unimportant factors that have a negligible impact on the results, the following reasonable assumptions are introduced when solving the steady-state temperature field of the 3-D IC model in this study:

- The contact thermal resistance between the two adjacent layers in 3-D IC is ignored, since the contact between the different layers is perfect and the materials are isotropic.

- The heat source is applied to the bottom end of each chip layer and the heat sink is attached to the upper end of the topmost chip. In other words, a heat source (0.1 W) is applied at the bottom of each chip layer and an isothermal boundary (such as 20 °C) is set on the upper surface of the topmost chip, based on boundary conditions from relevant literatures [10, 13].
- To better show the differences, only one variable is analyzed in a simulation. Thence, all the external surfaces in the simulation model except the hot side and the cold side are set as thermal isolation boundaries. The thermal conductivity of each material in the detailed 3-D IC is given in tab. 2 [39, 41].

**Table 2. Material properties**

Materials	Thermal conductivity [Wm <sup>-1</sup> K <sup>-1</sup> ]
Copper	390
Si	150
SiO <sub>2</sub>	1.5
Ni	60.7
Ni <sub>3</sub> Sn <sub>4</sub>	19.6
Sn <sub>2.5</sub> Ag	57
Underfill	0.2

### Equivalent thermal conductivity methods

Figure 2(a) shows a single TSV cell with pitch for the length and width of the cell and  $\Delta z$  for its height. The interior of the TSV is filled with copper, which is surrounded by a thin layer of silica. Since the thermal conductivity of copper is approximately 260 times higher than that of silica, which has a thermally insulating effect on TSV in the in-plane direction. Thus, the equivalent thermal conductivity in the in-plane and out-plane orientations must be computed individually [26]. The equivalent thermal conductivity of TSV in the out-of-plane direction,  $k_{eq-z}$ , can be deduced based on the parallel thermal resistance network model:

$$k_{eq-z} = k_{Cu} v_{Cu} + k_{SiO_2} v_{SiO_2} + k_{Si} v_{Si} \quad (2)$$

where  $v$  and  $k$  are the volume fraction and thermal conductivity of the material, respectively.

A combination of integral and series-parallel thermal resistance network models is proposed to solve the equivalent thermal conductivity of TSV in the in-plane direction. As shown in fig. 2(b), the model is symmetric in both the  $x$  and  $y$  directions, so only 1/4 of the model (upper right corner) needs to be calculated. The Cu and silica in the  $x$ -direction with lengths  $x_1$  and  $x_2$  in fig. 2(b) are represented:

$$x_1 = \sqrt{r_1^2 - y^2} \quad (3)$$

$$x_2 = \sqrt{r_2^2 - y^2} \quad (4)$$

where  $r_1$  and  $r_2$  are the radius of the copper and silica layer, respectively.

The 1/4 model (upper right corner) in fig. 2(b) can be divided into three parts, as shown in fig. 2(b). According to the series thermal resistance network model and the integration method, the thermal conductivity of Parts 1 and 2 are calculated, respectively:

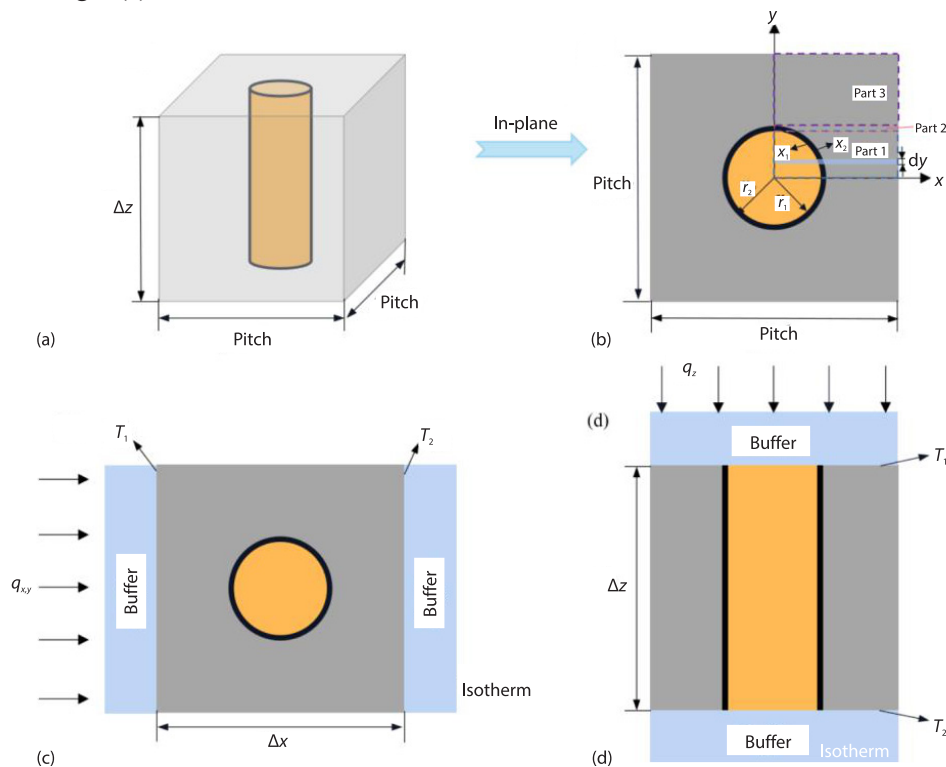
$$k_1 = \int_0^{r_1} \frac{1}{\frac{2x_1}{pitch \cdot k_{Cu}} + \frac{2x_2 - 2x_1}{pitch \cdot k_{SiO_2}} + \frac{pitch - 2x_2}{pitch \cdot k_{Si}}} dy \quad (5)$$

$$k_2 = \int_{r_1}^{r_2} \frac{1}{\frac{2x_2}{\text{pitch} \cdot k_{\text{SiO}_2}} + \frac{\text{pitch} - 2x_2}{\text{pitch} \cdot k_{\text{Si}}}} dy \quad (6)$$

Part 3 contains only silicon, which has a thermal conductivity of  $k_{\text{Si}}$ . According to the parallel thermal resistance network model, the equivalent thermal conductivity of the 1/4 model in the in-plane direction is derived:

$$k_{\text{eq-x,y}} = k_1 \frac{2r_1}{\text{pitch}} + k_2 \frac{2r_2 - 2r_1}{\text{pitch}} + k_3 \frac{\text{pitch} - 2r_2}{\text{pitch}} \quad (7)$$

The accuracy of the proposed analytical method in terms of in-plane and out-of-plane thermal conductivity is verified by performing finite element simulations on a detailed 3-D model of a single TSV unit, as shown in fig. 2. A uniform heat flow  $q_z$  ( $10^6 \text{W/m}^2$ ) is applied to the top surface of the model when extracting the out-of-plane equivalent thermal conductivity, and the bottom surface is set as a constant temperature boundary ( $20^\circ \text{C}$ ). The surrounding surface area is set as an adiabatic boundary. In addition, a buffer block is added at the entrance and exit of the heat flow model to make the simulation results more accurate, as shown in fig. 2(d). A similar operational set-up is used for extracting the in-plane thermal conductivity, as shown in fig. 2(c).



**Figure 2. Model for extracting the thermal conductivity of a single TSV unit; (a) detailed model of TSV unit, (b) thermal resistance network model for  $k_{x,y}$ , (c) 3-D FE model for  $k_{x,y}$ , and (d) 3-D FE model for  $k_z$**

The average temperatures  $T_1$  and  $T_2$  of cross-sections 1 and 2 are obtained from the simulation results. According to Fourier's law, the equivalent thermal conductivity of the TSV chip in both horizontal and vertical directions can be determined, respectively:

$$k_{x,y} = q_{x,y} \frac{\Delta x}{T_1 - T_2} \quad (8)$$

$$k_z = q_z \frac{\Delta z}{T_1 - T_2} \quad (9)$$

Assume that the TSV cell has  $r_1$  of 8  $\mu\text{m}$ ,  $r_2$  of 9  $\mu\text{m}$ , pitch of 40  $\mu\text{m}$ , and  $\Delta x$  and  $\Delta z$  of 40  $\mu\text{m}$ , the in-plane equivalent thermal conductivities calculated by the proposed analytical and FEM are 116.74 W/mK and 115.3 W/mK, respectively. For the equivalent thermal conductivity in out-plane direction, the results of the analytical and FEM are 175.2 W/mK and 169.6 W/mK, respectively. The error of in-plane and out-of-plane equivalent thermal conductivities values calculated by the two methods is only 1.2% and 3.9%, respectively, which proved the accuracy of the proposed analysis method.

As shown in fig. 1(a), all microbumps are a laminate structure consisting of continuous phases. According to the series and parallel thermal resistance network models, the equivalent thermal conductivities of micro-bumps in the out-of-plane and in-plane directions are solved, respectively:

$$k_{\text{eq},z} = \frac{1}{\sum_{i=1}^n \frac{v_i}{k_i}} \quad (10)$$

$$k_{\text{eq},x-y} = \sum_{i=1}^n k_i v_i \quad (11)$$

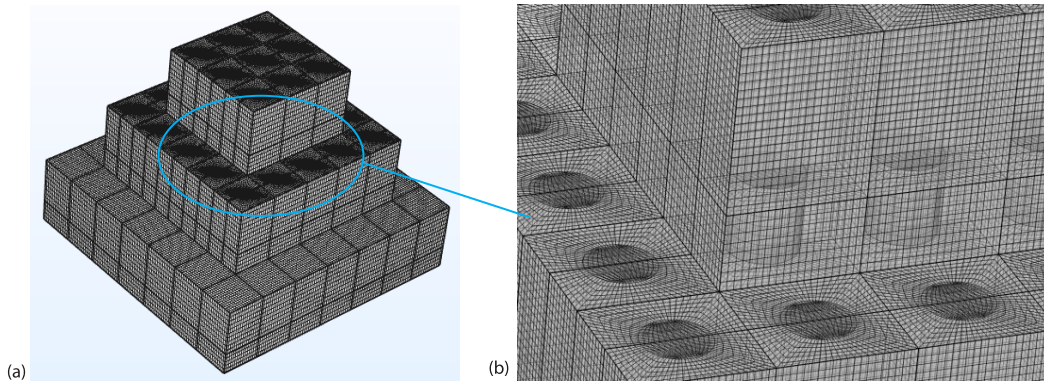
where  $k_i$  ( $i = 1, 2, \dots, n$ ) represents the thermal conductivity of the  $i^{\text{th}}$  layer of material, and  $v_i$  ( $i = 1, 2, \dots, n$ ) denotes the volume fraction of the  $i^{\text{th}}$  layer of material, where  $v_i$  satisfies  $\sum v_i = 1$ .

### Grid independence

To validate the reliability of the thermal analysis procedure for 3-D IC, the model is firstly divided into structured meshes, as shown in fig. 3. The structured hexahedral mesh was chosen because it has lower mesh numbers and higher mesh quality than the software's automatic tetrahedral meshing. The diameter, pitch of TSV and  $\text{SiO}_2$  layer thickness in the simulation were 16  $\mu\text{m}$ , 40  $\mu\text{m}$ , 1  $\mu\text{m}$ , respectively. In addition, all meshes are hexahedral structures, and the minimum and average quality of the overall meshes are 0.67 and 0.84, respectively, which indicates that the selected meshes fully meet the requirements of steady-state thermal analysis. Meanwhile, due to the heavy computational task, it is necessary to determine the appropriate grid size before numerical calculation. Since temperature is one of the most important metric in thermal management of 3-D IC, the maximum temperature of each layer chip is chosen as the goal indicator.

Figure 4 shows the numerical results for the maximum temperature variation of each layer chip with five different grid numbers. The results demonstrated that the temperature increases slowly when the number of grids is less than 2 million and then keeps the maximum temperature almost unchanged with the increase of the grid. Furthermore, the maximum tem-





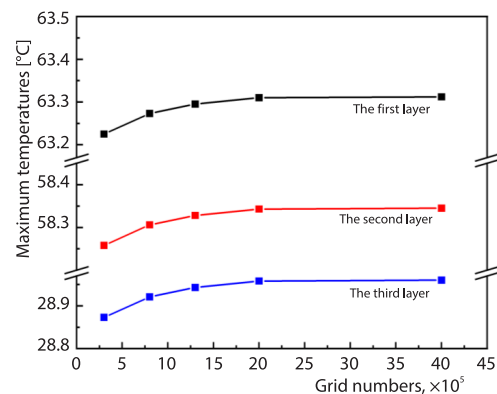
**Figure 3.** The selected model meshes; (a) overall view of the grid and (b) partial enlargement of the grid

perature variation range of each layer chip under five different grid numbers is less than 1%, which indicates that the simulation results of the 3-D IC model were independent of the grid. Therefore, 2000000 hexahedral mesh is selected as the grid system of FEM to calculate the temperature profile, which can remarkably reduce computational cost while ensuring computational accuracy.

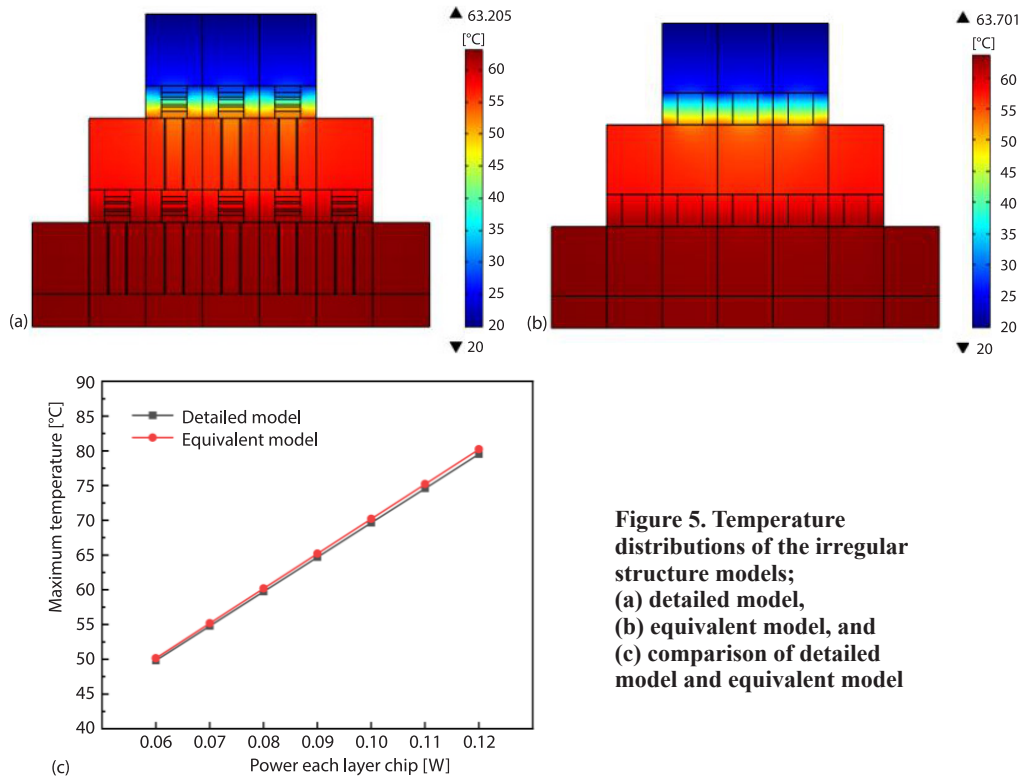
### Results and discussion

To evaluate the validity of the equivalent model in the thermal analysis of 3-D IC, a detailed model and an equivalent model of irregularly structured 3-D IC are built, respectively. In the simulation, a heat source with uniform power (0.087 W) is applied at the entire bottom surface of each layer chip. The diameter, pitch of the TSV and SiO<sub>2</sub> layer thickness on the chip are 16 μm, 40 μm, and 1 μm, respectively. Detailed parameters for each structure and material are shown in tabs. 1 and 2. Figures 5(a) and 5(b) exhibit the temperature distributions and temperature gradient contours of the detailed and equivalent model, respectively. Figure 5(c) shows the comparison of detailed model and equivalent model under different powers. The results demonstrate that the temperature distribution obtained from the equivalent model is in perfect agreement with the detailed model under the same condition. Maximum temperature deviation between the equivalent and detailed models is less than 1%, and computation time for the detailed model and the equivalent model is 10 minutes and 2.7 minutes, respectively. Therefore, there is reason believe that the equivalent model is fully feasible in thermal analysis of irregularly structured 3-D IC, in which computation time can be significantly reduced compared to that of the detailed model.

The distribution and power of the heat source directly affect the maximum temperature and the performance of 3-D IC. Moreover, structural parameters of TSV also affect heat transport between adjacent layers, which may further deteriorate the temperature distributions. Therefore, a comprehensive analysis of the influence of these parameters on key indicators, especially the maximum temperature is implemented in this section. In order to save compu-



**Figure 4.** Grid independence test



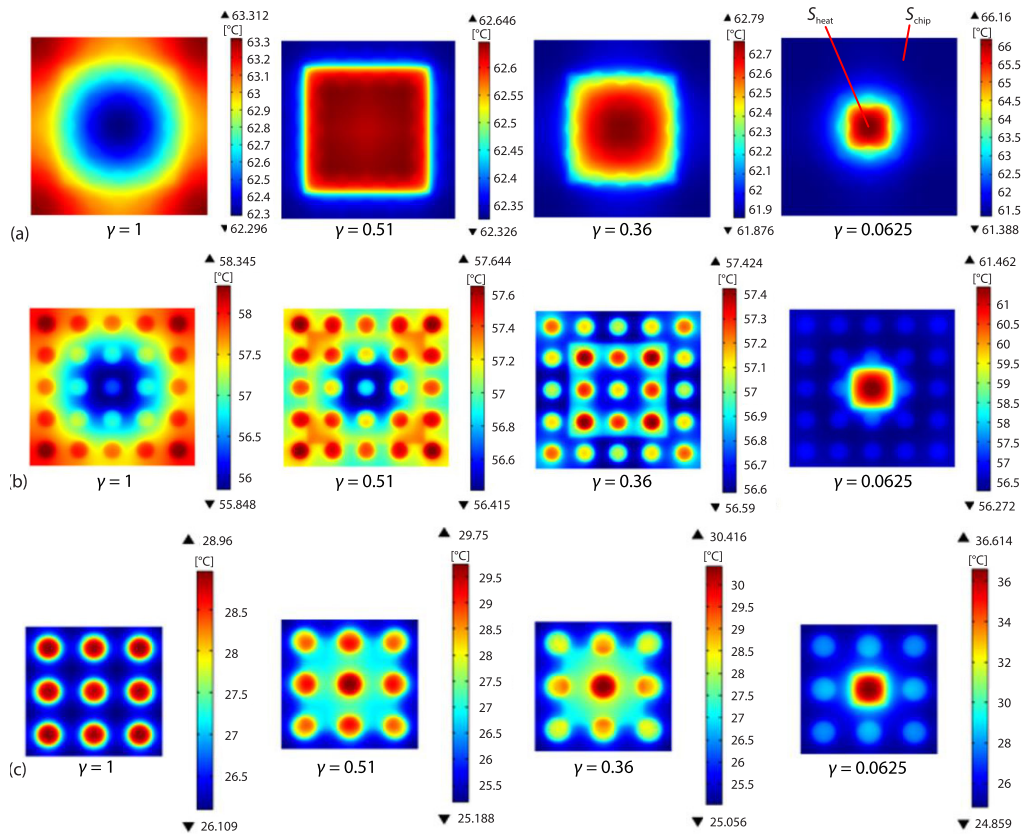
**Figure 5. Temperature distributions of the irregular structure models; (a) detailed model, (b) equivalent model, and (c) comparison of detailed model and equivalent model**

tational cost, the effects of the relevant parameters on the thermal performance of irregularly structured 3D IC are investigated based on the equivalent model.

#### Heat source area

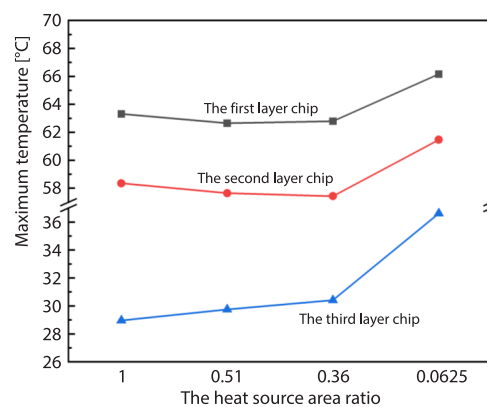
Figure 6 shows the steady-state temperature distribution of each chip heat source surface under different heat source area ratios  $\gamma$ . The heat source  $\gamma$  is the ratio of the area of the heat source on that layer of the chip to the area of the chip,  $\gamma = S_{\text{heat}}/S_{\text{chip}}$ . In the simulation, a heat source with unified power (0.1 W) is applied at the center of each layer of the chip, the diameter and pitch of the TSV on the chip are 16  $\mu\text{m}$  and 40  $\mu\text{m}$ , respectively. Simultaneously, the thickness of the  $\text{SiO}_2$  is 1  $\mu\text{m}$ . As it can be seen in fig. 6(a), the maximum temperature of the first layer (bottom) chip is minimized when the heat source area ratio is 0.51. In addition, when a uniform heat source is applied, the maximum temperature occurs at the four corners of the bottom chip. Conversely, the maximum temperature of the third layer (top) chip encircles the TSV when the heat source area ratio is 100%, as shown in fig. 6(c). The highest hot spot temperature will appear when the heat source area is the smallest ( $\gamma = 0.0625$ ). Figure 7 shows the effect of the heat source area ratio on the maximum temperature of each layer in the 3-D IC with irregular structures. The results reveal that the maximum temperature of the first and the second layer chip first decreased slowly and then increased significantly with the decrease of the heat source area ratio. This is because the large size chip has TSV only in the part that completely overlaps with the upper layer chip. When the heat source area is reduced to be exactly equal to the area of the overlapping area ( $\gamma = 0.51$ ), this area just fits the TSV area with high out-plane thermal conductivity, so the maximum temperature is minimized. When





**Figure 6. Steady-state temperature distribution of each layer chip with different heat source area ratios; (a) the first layer chip, (b) the second layer chip, and (c) the third layer chip**

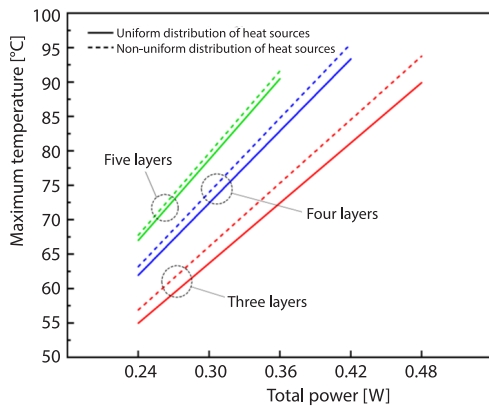
the heat source area gradually decreases in the TSV area, the heat source is more concentrated, resulting in an increase in power density, and the heat flow cannot be diffused in time, so the maximum temperature will increase significantly. In addition, it can also be seen that the maximum temperature of the third layer increases with the decrease of the heat source area ratio. This is because the third layer chip connect directly to the heat sink. The reduction of the heat source area leads to an increase in the power density, so the maximum temperature will increase. Therefore, the heat source area of the large chip containing TSV is exactly equal to the area of the small chip on the upper layer, which is the best heat source area to improve the heat transfer performance.



**Figure 7. Maximum temperature of each layer chip with different heat source area ratio**

### Total power

Figure 8 shows the effect of the total power and the number of chip layers on the maximum temperature of 3-D IC with irregular structures. The uniform heat source ( $\gamma = 1$ ) and non-uniform heat source ( $\gamma = 0.0625$ ) are investigated, respectively. In the simulation, the total power is uniformly applied on each layer chip, and the diameter and pitch of TSV are  $16 \mu\text{m}$  and  $40 \mu\text{m}$ , respectively. Simultaneously, the thickness of  $\text{SiO}_2$  is  $1 \mu\text{m}$ . The sizes of the 5-layer chip from bottom to top are  $440 \mu\text{m} \times 440 \mu\text{m}$ ,  $360 \mu\text{m} \times 360 \mu\text{m}$ ,  $280 \mu\text{m} \times 280 \mu\text{m}$ ,  $200 \mu\text{m} \times 200 \mu\text{m}$ , and  $120 \mu\text{m} \times 120 \mu\text{m}$ , respectively. As it can be seen in fig. 8, the maximum temperature of 3-D IC increases linearly with the increase of the total power. If the maximum allowable working temperature is  $90 \text{ }^\circ\text{C}$ , the total permitted power of 3-D IC will decrease as the number of layers increases. In addition, it can also be seen that the difference of the maximum temperature between uniform and non-uniform distributed heat sources increases slowly with the increase of the total power. This is because the hot spot effect becomes more pronounced as the total power increases, which leads to an increase in temperature difference. Furthermore, temperature difference between uniform and non-uniform distributed heat sources decreases slowly with the



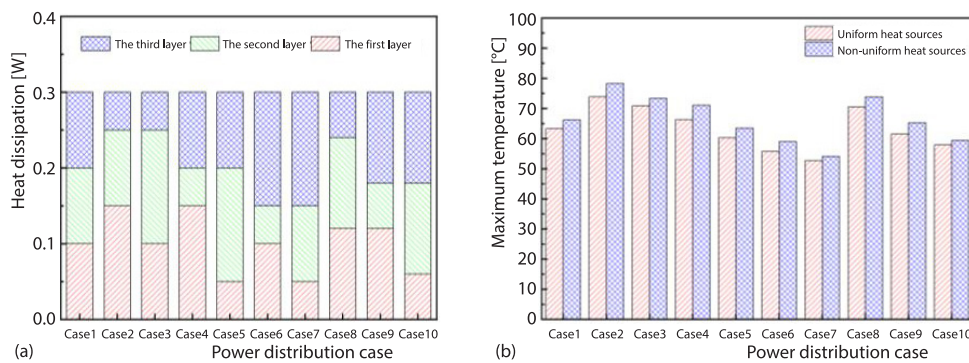
**Figure 8. Maximum temperature of each layer chip with different heat source area ratio**

### Power setting

Figure 9 shows a detailed case study evaluating the dependence of the maximum temperature on the power magnitude of the heat source area on the chip at each layer. After determining the total power of the model to be  $0.3 \text{ W}$  through section *Total power*, it is unknown how to distribute the total power to each layer of the chip and the best way to do so. The same power was assumed in most studies for the heat source region on each layer of the chip. However, the fact is that the total power dissipated on each functional chip layer is not necessarily uniform, and the power on each chip layer may not be equal. In this work, the power distribution of the three-layer 3-D IC is divided into three categories. The first category (Case 1) is that the power of each layer chip is equal, the second category (Case 2-Case 7) is that the power of each layer is not equal, and the third category (Case 8-Case 10) is that two of the three-layer chips have the same power. To facilitate the analysis, the power of the chip is set to high, medium and low levels, and the values are multiplied, as shown in tab. 3 and fig. 9(a). Figure 9(b) shows the effect of the power of each layer chip on the maximum temperature of the 3-D IC with irregular structures under uniform heat source ( $\gamma = 1$ ) and non-uniform heat source

increase of the stacked layers. This is because the hot spot effect becomes more pronounced with the increase of the total power, resulting in an increase of the temperature difference. On the contrary, the power and power density of each chip decreases as the number of chip layers increases. This is because the increase in the number of layers leads to a higher degree of integration heat is not easily dissipated, and thus the need to reduce the power of each layer of the chip to control the maximum temperature does not exceed the temperature threshold. Therefore, the analysis of the total power is a prerequisite for the reasonable setting of the power of each layer, and the total power of the three layers of chips is determined to be  $0.3 \text{ W}$ .

( $\gamma = 0.0625$ ). The results demonstrate that maximum temperature difference in Cases 2 and 7 under uniform and non-uniform heat source reach 21.15 °C and 24.14 °C, respectively. Moreover, the difference of maximum temperature between Cases 8 and 10 under uniform and non-uniform heat source is 12.69 °C and 14.48 °C, respectively. It can also be seen that for the second type of power distribution Case 7 is the best power setting and for the third type of power distribution Case 10 is the best power setting. That is to say that increasing/reducing the power of the chip close to/farther away from the heat sink can reduce the maximum temperature of 3-D IC, perfectly consistent with the results of Tavakkoli *et al.* [11]. Our research work provides a useful reference for power settings of each layer in 3-D IC with irregular structures.



**Figure 9. Maximum temperature with different power distribution;**  
**(a) case of power distribution in each layer chip and**  
**(b) effect of the power distribution cases on maximum temperature**

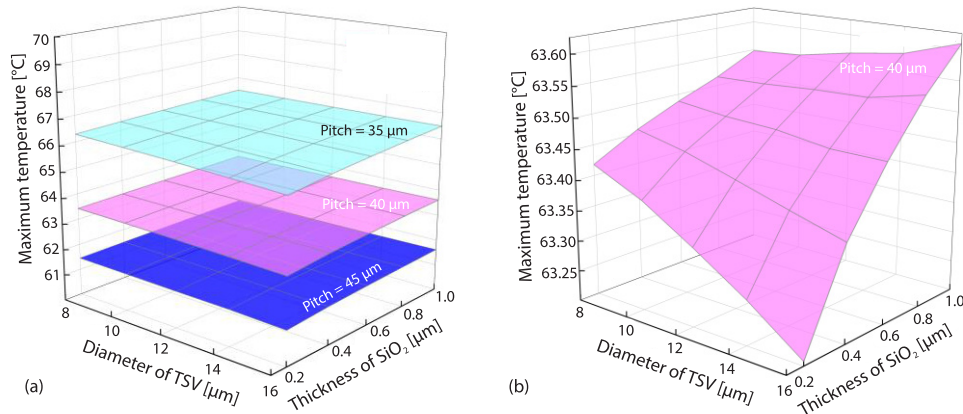
**Table 3. Case of power distribution of each chip in the three-layer chip**

Categories	Cases	Power of the first layer of chips [W]	Power of the second layer of chips [W]	Power of the third layer of chips [W]
The first category	Case 1	0.1	0.1	0.1
The second category	Case 2	0.15	0.1	0.05
	Case 3	0.1	0.15	0.05
	Case 4	0.15	0.05	0.1
	Case 5	0.05	0.15	0.1
	Case 6	0.1	0.05	0.15
	Case 7	0.05	0.1	0.15
The third category	Case 8	0.12	0.12	0.06
	Case 9	0.12	0.06	0.12
	Case 10	0.06	0.12	0.12

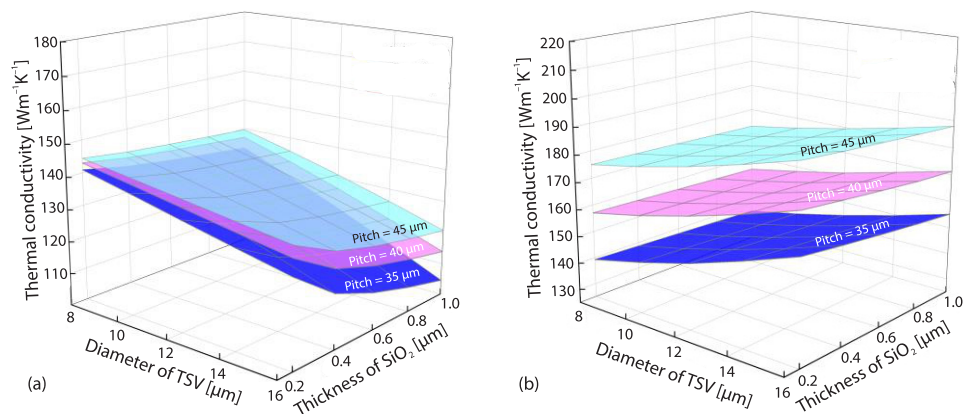
*The TSV structural parameters*

Figure 10(a) shows the effect of TSV structure parameters (TSV pitch, TSV diameter and SiO<sub>2</sub> thickness) on the maximum temperature of 3-D IC with irregular structure. The results illustrate that among the TSV structural parameters, the TSV pitch has a significant influence on the maximum temperature, which increases with the decrease of the pitch of TSV. This is because the pitch of TSV has a significant effect on the volume fraction of TSV is in the chip,

which directly affects the equivalent thermal conductivity of TSV chip, as shown in fig. 11. Since the trends of the TSV parameters on the maximum temperature under different pitches are consistent, the TSV pitch of  $40\ \mu\text{m}$  is selected as a typical case for enlarged analysis, as shown in fig. 10(b). It can be seen that the maximum temperature of 3-D IC shows two different trends with the increase of  $\text{SiO}_2$  thickness and TSV diameter. When the  $\text{SiO}_2$  thickness ranges from  $0.2\text{-}0.6\ \mu\text{m}$ , the maximum temperature decreases with the increase of TSV diameter. On the contrary, the maximum temperature increases with the increase of TSV diameter when the  $\text{SiO}_2$  thickness is greater than  $0.6\ \mu\text{m}$ . In other words, there is a watershed of  $\text{SiO}_2$  thickness values, which affects the relationship between the TSV diameter and the maximum temperature. This is caused by the variation in the thermal conductivity of TSV structural parameters, as shown in fig. 11. Figure 11(a) and 11(b) show the in-plane and out-plane equivalent thermal conductivity of TSV chip with different structural parameters. Specifically, the out-plane thermal conductivity of TSV chip increases with the increase of TSV diameter when the thickness of  $\text{SiO}_2$  ranges from  $0.2\text{-}0.6\ \mu\text{m}$ . The in-plane thermal conductivity reduces with the increase of the TSV diameter when the thickness of  $\text{SiO}_2$  is greater than  $0.6\ \mu\text{m}$ , as shown in fig. 11(a). Therefore, the TSV pitch is a significant parameter to improve the thermal performance of 3-D IC with irregular structures.



**Figure 10. Effect of TSV structural parameters on the maximum temperature; (a) three different TSV pitches and (b) pitch =  $40\ \mu\text{m}$**



**Figure 11. Equivalent thermal conductivity of different TSV structural parameters; (a) in-plane and (b) out-plane**



## Conclusions

In this paper, a detailed model of a tight three-layer 3-D IC with irregular structure considering TSV and micro-bumps is proposed, and an analytical method to accurately extract the equivalent thermal conductivity of 3-D IC is presented. Thermal performance of irregularly structured 3-D IC are numerically studied based on the equivalent model. The key results, are as follows.

- An analytical method based on the thermal resistance network model is proposed to extract the equivalent thermal conductivities of TSV and micro-bumps, the accuracy of which is verified by 3-D finite element simulations.
- The optimal heat source area of each layer containing TSV is equal to the size of the overlap area between the chip and adjacent small one.
- High power chip close to heat sink can minimize the maximum temperature of 3-D IC, regardless of the chip size.
- Different TSV structural parameters have different sensitivities to the maximum temperature of 3-D IC. A smaller TSV diameter and TSV pitch and a larger SiO<sub>2</sub> thickness would raise the maximum temperature of TSV chips.
- When the TSV pitch is 40 μm, there is a watershed of SiO<sub>2</sub> thickness,  $t$ , value ( $t = 0.6 \mu\text{m}$ ), which affects the relationship between TSV diameter and maximum temperature.
- When optimizing TSV structure parameters, it is recommended to reduce the TSV pitch for thermal management of 3-D IC with irregular structure.

Although this paper provides some insights into the thermal modelling and optimal design of irregularly structured 3-D IC, the proposed models are still small and may not be representative in practical problems. Therefore, it is necessary to further generalize to numerical studies on more practical and larger chips, such as Intel Lakefield chip.

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