# OPTIMIZED METHOD FOR THERMAL THROUGH SILICON VIA PLACEMENT WITH NON-UNIFORM HEAT SOURCES IN 3-D-IC

by

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*In the past few years, thermal through silicon via (TTSV) has been experimentally investigated as an effective heat dissipation path. Although a lot of heat dissipation-related issues have been solved in 3-D integrated circuit (3-D-IC), there are neglections in TTSV placement with non-uniform heat sources so far. In this study, a unique optimization is proposed to locate TTSV while effectively alleviating hot spots in 3-D-IC. The thermal dissipation of non-uniform heat sources are studied using the finite element method. The simulation results show that the minimum temperature is reduced by 2.1% compared with peak temperature in the single-layer chip, and by 1.9% in the three-layer chip.*

Key words*: 3-D integrated circuit, non-uniform, optimized method, cost function, thermal through silicon via*

## Introduction

The application of a stacked 3-D-IC has offered significant improvements in the system integration and packaging density, but the overheated hot spot problem remains a key issue in chip manufacturing and operation [1, 2]. The technology of 3-D-IC based on TSV can effectively and quickly facilitate heat transfer and reduce the power consumption of chips [3]. Thermal management is considered as an extremely complex challenge in 3-D-IC development [4]. Compared with traditional 2-D integrated circuit, thermal management of 3-D-IC is more urgent, while the device performance, reliability and lifespan must be maximized [5-7].

More beneficial methods for better heat dissipation in thermal management are required to address the thermal challenges in 3D-IC. In the vertical direction of the 3-D-IC, effective utilization of a heat dissipation channel with TTSV is a vital factor to be considered [8, 9]. Goplen and Sapatnekar in [10], introducing TTSV into 3-D-IC is a promising way to alleviate thermal problems by reducing the effective thermal resistance of the chip. Sheng *et al.* in [11], transient thermal simulation of a 3-D integrated circuit was proposed. With an assumption of vertical and lateral heat transfer of 3-D-IC in [12], a numerical model of the equivalent, the anisotropic thermal conductivity was researched. Ma *et al.* in [13], the effect of TSV arrangement on transmission performance was analyzed. Rakesh *et al.* in [14], a method of reducing the temperature by adding the heat sink to the TTSV in 3-D-IC was proposed.

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Therefore, limited by the technical and economic difficulties in 3-D-IC size scaling technology, the method of optimizing TTSV placement becomes particularly valuable [15]. Budhathoki *et al.* in [16], an efficient 3-D multilevel routing approach was proposed, which included a novel TTSV planning method. A fixed-outline 3-D floorplanning was proposed by the implementation of a quick thermal analysis method in [17]. Ren *et al.* in [18], an optimized method was proposed to optimally place TTSV between IC blocks compared to floor plans with a fixed TTSV lay-out. Considering various TSV failure mechanisms and workloads in [19, 20], a framework was presented with awareness of TSV lifetime reliability. Radeep *et al.* in [21], a new optimization method is proposed for useful partitioning, placing, and routing is proposed. However, the method for inserting TTSV in chips with non-uniform heat sources, with limited space, was still not widely studied.

In this study, we present a mathematical analytical method based on the cost function of 3-D-IC for the rapid localization of TTSV. The method is numerically analyzed and verified by MATLAB software. Compared with the COMSOL simulations, our proposed mathematical thermal method can complete TTSV placement rapidly in non-uniform heat sources. Furthermore, this method is feasible and easy to calculate.

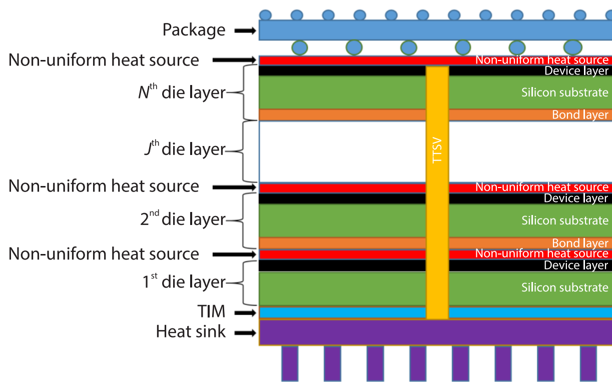


**Figure 1. A general 3-D-IC structure with TTSV**

## Methodology

The analytical thermal model of 3-D-IC is displayed in fig.1, where TTSV is integrated into the physical structure. The heat flow in the lateral direction within the layer is generated from non-uniform heat sources. Considering the low thermal conductivity of each bond layer, the thermal transmission of the inter-layer is difficult and assumed to be neglected in the vertical direction. On the other hand, TTSV with high thermal conductivity filler material can transfer the heat of inter-layer from the top layer to heat sink in the bottom layer in the vertical direction.

Instead of the general assumption that power is uniformly distributed on each chip, in this paper, non-uniform heat sources are introduced in line with real applications. Here only one layer of the overall structure is analyzed, the non-uniform heat sources are acquired randomly. Figure 2(a) charts the top view of the geometric configuration of non-uniform heat sources in diverse colors, which represent the various amount of power density. Each cell is modelled with thermal properties in the lateral direction, plotted in fig. 2(b). $\text{Cell}_{j,x1,y1}$ and $\text{Cell}_{j,x,y}$ represent the cell where TTSV is located and one of the other cells, respectively.

To simplify the thermal behavior in 3-D-IC, a 2-D equivalent thermal resistance model based on non-uniform heat sources is developed in fig. 3(a). Taking the $j^{\text{th}}$ layer for example, when TTSV is placed at a co-ordinate of $(x_1,y_1)$, $Q_{j,x,y}$ is the heat generated from the $j^{\text{th}}$ device layer of the $\text{Cell}_{j,x,y}$. The $T_{j,a}$ and $T_{j,b}$ are the temperature of the $\text{Cell}_{j,x,y}$ and $\text{Cell}_{j,x1,y1}$, respectively. The $T_{j,\text{TTSV}}$ is the temperature of TTSV. The $R_{j,\text{x,y}}$ is the lateral thermal resistance between the $\text{Cell}_{j,x,y}$ and $\text{Cell}_{j,x1,y1}$. The $R_{\text{j,x1,y1}}$ represents the lateral thermal resistance of the $j^{\text{th}}$ isolation dielectric layer. The $R_{j,\text{TTSV}}$ represents the thermal resistance of TTSV in the $j^{\text{th}}$ device layer. From Kirchhoff's current Law (KCL), it can be obtained:

$$\sum Q_{j,x,y} + \sum \frac{T_{j,a} - T_{j,b}}{R_{j,x,y}} = \frac{T_{j,\mathrm{TTSV}} - T_{j-1,\mathrm{TTSV}}}{R_{j,\mathrm{TTSV}}} - \frac{T_{j+1,\mathrm{TTSV}} - T_{j,\mathrm{TTSV}}}{R_{\mathrm{j+1,TTSV}}} \tag{1}$$

where

$$\left( \sum Q_{j,x,y} + \sum \frac{\mathrm{T}_{j,a} - \mathrm{T}_{j,b}}{R_{j,x,y}} \right)$$

is the lateral heat flow of the $j^{\mathrm{th}}$ layer, while

$$\frac{T_{j,\mathrm{TTSV}} - T_{j-1,\mathrm{TTSV}}}{R_{j,\mathrm{TTSV}}} \text{ and } \frac{T_{j+1,\mathrm{TTSV}} - T_{j,\mathrm{TTSV}}}{R_{j+1,\mathrm{TTSV}}}$$

is the vertical heat flow of the $j^{\mathrm{th}}$ and $(j-1)^{\mathrm{th}}$ layer, respectively.

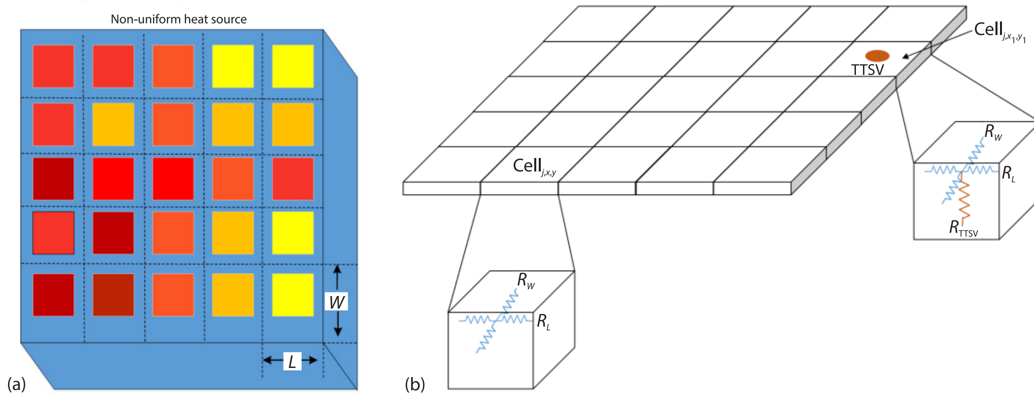


**Figure 2. The top view of 3-D-IC with non-uniform heat sources**

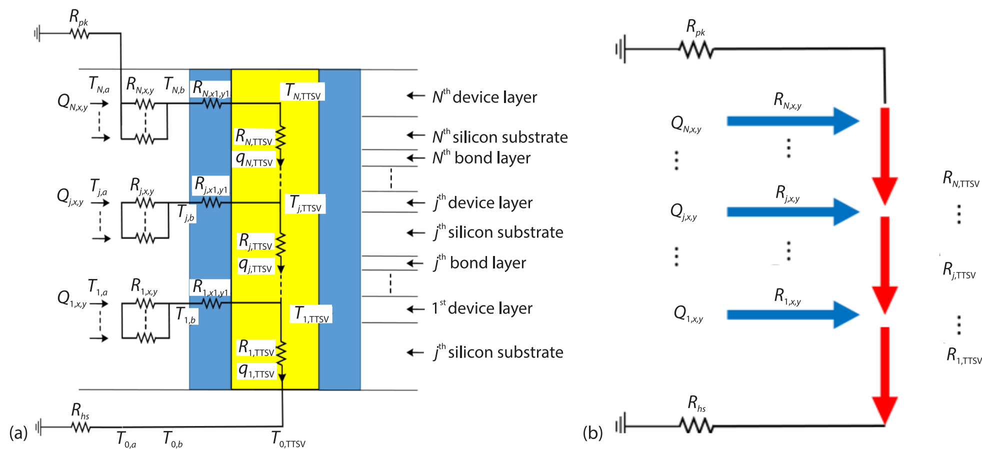


**Figure 3. The equivalent thermal resistance model of 3-D-IC with non-uniform heat sources**

Figure 3(b) illustrates the main heat flow both in the lateral direction and vertical direction. When the heat source is located at a higher layer of $Z$ with a higher lateral thermal resistance of $R_{j,x,y}$, and packed with more dissipated power of $Q_{j,x,y}$, the temperature rise between the

top layer and the bottom one will go higher. Due to the diverse dimension of $Z$, $R_{j,x,}$, and $Q_{j,x,y}$, the normalized layer of the chip, the lateral thermal resistance and the heat flow are introduced.

It is defined that $Q_{max}$ is the maximum of heat flow in the lateral direction. The $R_{max}$ is the maximum of lateral thermal resistance between $\text{Cell}_{j,x,y}$ and $\text{Cell}_{j,x1,y1}$. The $Z_{max}$ is the total layers of the whole chip. In the normalization, $Q_{nor}$ is the factor of heat flow, Rnor is the factor of thermal resistance, and $Z_{nor}$ is the factor of layers:

$$Q_{nor} = \frac{Q_{j,x,y}}{Q_{max}} \tag{2}$$

$$R_{nor} = \frac{R_{j,x,y}}{R_{max}} \tag{3}$$

$$Z_{nor} = \frac{Z}{Z_{max}} \tag{4}$$

The cost function is expressed:

$$F_{cost=} \sum\sum\sum Q_{nor} R_{nor} Z_{nor} = \sum_{j=1}^{N}\sum_{x=1}^{m}\sum_{y=1}^{m} \frac{Q_{j,x,y}}{Q_{max}} \frac{R_{j,x,y}}{R_{max}} \frac{Z_{j,x,y}}{Z_{max}} \tag{5}$$

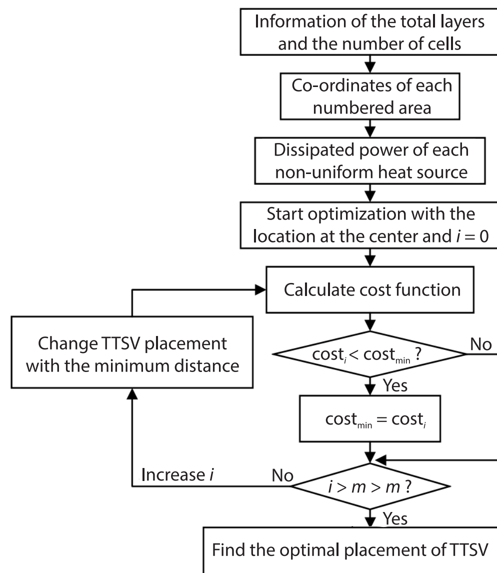


**Figure 4. Optimization flow of TTSV placement**

The objective of the cost function is to find a feasible method for the TTSV optimized placement to facilitate heat transfer in 3-D-IC. From eq. (5), it can be obtained that the lower the cost, the better the thermal performance will be in 3-D-IC with TTSV placement.

The minimum cost determines the location of TTSV in the light of the non-uniform heat distribution of all layers. The whole optimization flow is displayed in fig. 4 with calculations:

Step 1 – Information of the total layers $N$, and the number of cells in each layer $m \times m$.

Step 2 – Co-ordinates of each numbered area ($x$, $y$, $z$), which represent the location at the center of the area in the $Z^{th}$ layer.

Step 3 – The dissipated power of each non-uniform heat source, which is generated randomly and saved in $Q$ expressed as: $Q_{j,1,1}$, $Q_{j,1,2}$,... $Q_{j,x,y}$, $Q_{j,m,m}$.

Step 4 – It is assumed that TTSV is located at $P_i$ which is the center of non-uniform heat sources. Cost function of eq. (5) is calculated and stored as $\text{cost}_{min}$.

Step 5 – Change TTSV placement from $P_i$ to $P_{i+1}$with the minimum distance. Cost function is calculated as $\text{cost}_{i+1}$. If $\text{cost}_{i+1} < \text{cost}_{min}$, $\text{cost}_{i+1}$ is stored as $\text{cost}_{min}$.

Step 6 – When $i \leq m \times m$, calculation of Step 5 is conducted repeatedly.

Step 7 – Otherwise (when $1 > m \times m$), $P_i$ with the minimum cost is the optimal placement of TTSV.

## Results and discussion

In this section, numerical calculations of the proposed optimized method were conducted in MATLAB on single-layer and three-layer stacked chips, respectively. Experimental results were validated with COMSOL 5.4 simulations in order to make the evaluation for the thermal performance of TTSV in 3-D-IC.

Heat sources are assumed to be distributed over each layer non-uniformly, with a total dissipated power of 0.005 W, the non-uniform heat sources are acquired randomly. Each layer is made up of 25 uniform sections with varying heat distributions, as diagrammed in figs. 5 (a)-5(c), which indicate the heat distribution of the chip's first, second, and third layers, respectively. As seen in fig. 5(d), these uniform areas in each layer are numbered.

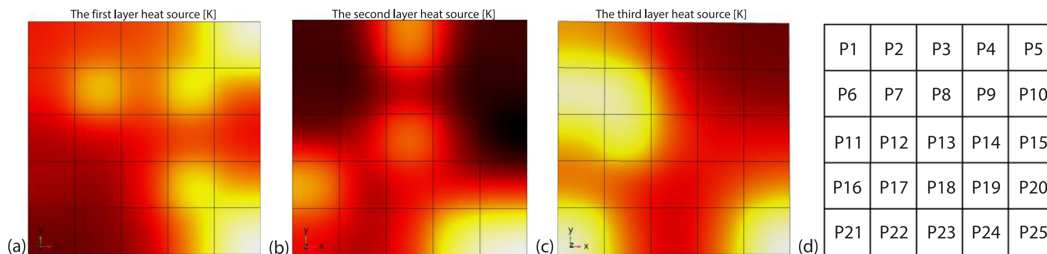


**Figure 5. Non-uniform heat sources; (a) the first layer, (b) the second layer, (c) the third layer, and (d) schematic with 25 numbered areas**

### *Numerical results of cost function*

According to figs. 6(a) and 6(c), numerical results of cost functions can be obtained by MATLAB when the TTSV is placed at the previous 25 numbered areas in the case of single-layer and three-layer, respectively. It indicates that the value of cost functions is lower when TTSV is placed around the hotspot of the chip. Hence, TTSV can be optimally placed at the hotspot of P14 in the single-layer case and P13 in three-layer case.

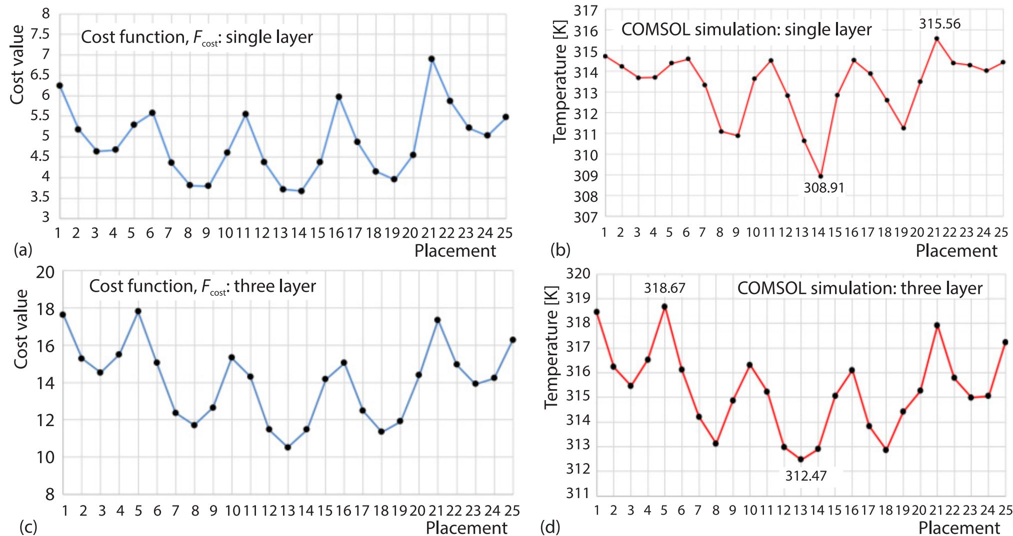


**Figure 6. Comparisons between the proposed method and COMSOL simulations; (a) numerical results of cost function in single-layer, (b) simulations in single-layer, (c) numerical results of cost function in three-layer, and (d) simulations in three-layer**

The experimental results show that the maximum temperature of a single-layer chip is 315.56 K, while the minimum is 308.91 K(P14) reduced by 2.1%, which is depicted in fig. 6(b). In the case of a three-layer from fig. 6(d), the maximum temperature is 318.67 K, while the minimum is 312.47 K (P13), which is reduced by 1.9%.

Compared with the proposed method and COMSOL simulations, it denotes that heat distribution relies heavily on the placement of TTSV, as peak temperature decreases significantly after optimization. The aforementioned analysis and validation show excellent agreement between the value of cost function and the temperature curves.

## *Thermal simulations of TTSV*

### *Thermal simulations on various positions of TTSV*

In the case of single-layer, models of 25 areas with non-uniform heat sources are all established by COMSOL as a square of 30 μm × 30 μm. Heat sources with a thickness of 0.1 μm, are covered at the upper surface of the overall structure while other boundaries are set to be adiabatic. The TTSV is one cylindrical copper with a diameter of 6 μm and a height of 50 μm to provide a vertical channel for alleviation of heat flow.

To investigate the relationship between temperature rise and position of TTSV, here, the radius of TTSV is constant and of the same filler material. Five positions around the centre of the chip are selected as placement of TTSV, which are P8, P12, P13, P14, and P18. Transient temperature fields are demonstrated in figs. 7(a)-7(e), with minimum peak temperature at P14.

Similarly, in the case of three-layer, transient temperature fields are obtained from Figs. 8(a)-8(e) when TTSV is settled at the positions of P7, P9, P13, P17, and P19. The peak temperature can be reduced at P13 near the critical hotspot of the chip. Consequently, the optimization for the placement of TTSV can achieve better thermal performance in 3-D-IC.

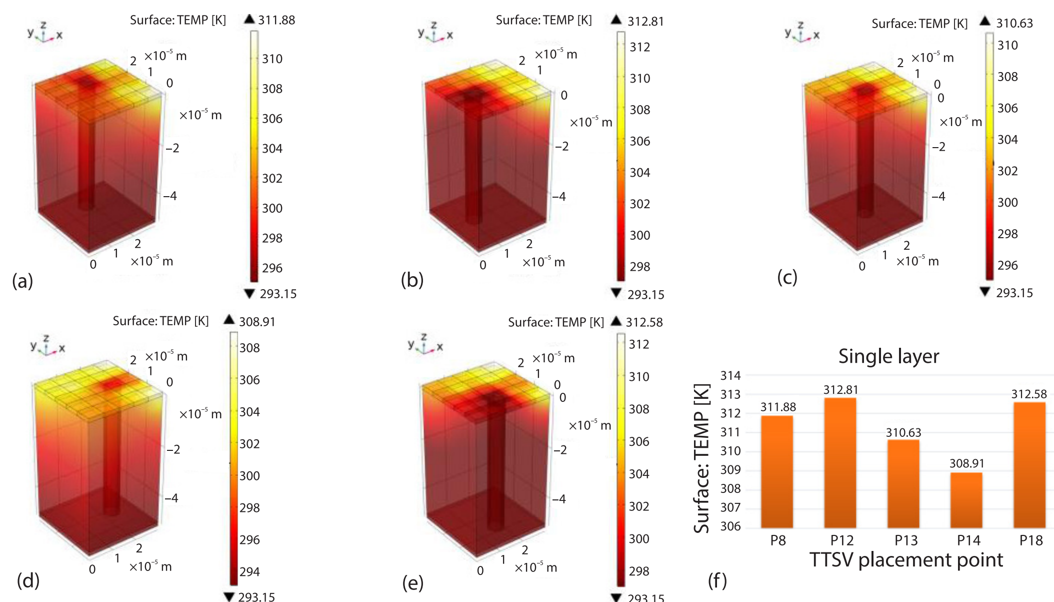


**Figure 7. Transient temperature fields in single-layer with various positions of TTSV at time $t$ = 1 second; (a) P8, (b) P12, (c) P13, (d) P14, (e) P18, and (f) peak temperatures of all the previous cases**

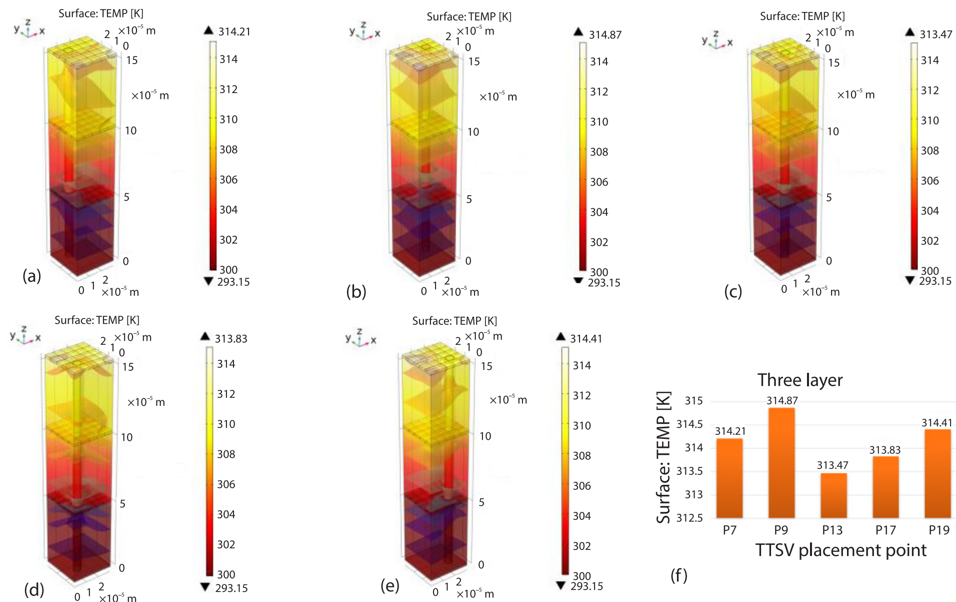


**Figure 8. Transient temperature fields in three-layer with various positions of TTSV at time $t$ = 1 second; (a) P7, (b) P9, (c) P13, (d) P17, (e) P19, and (f) peak temperatures of all the aforementioned cases**

## *Thermal simulations on various numbers of TTSV*

The effects of concentration of TTSV placement on temperature rise are further studied, dividing TTSV into one, two, three and four units, respectively. With the same total volume, the case of a single TTSV in fig. 9(a) can perform better than that in figs. 9(b)-9(d). Simulation results show that the more concentration of TTSV, the better heat dissipates.

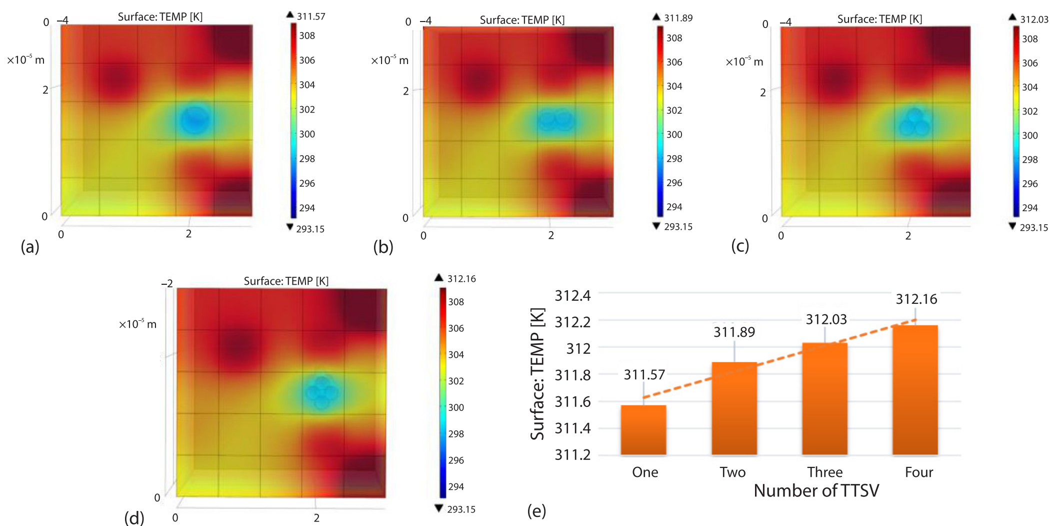


**Figure 9. Transient temperature fields in single-layer with various numbers of TTSV at time $t$ = 1 second; (a) 1, (b) 2, (c) 3, (d) 4, and (e) peak temperatures of all the cases mentioned previously**

### *Thermal simulations on various filler materials of TTSV*

To extend the analysis, TTSV is set at the co-ordinate of P14 with the same radius, while filled with various materials of the Al, Cu, CNT, and graphene nanoribbon (GNR), respectively. The thermal conductivity of the four filler materials is 237 W/mK, 397 W/mK, 2980 W/mK, and 5300 W/mK. The corresponding peak temperatures of the aforementioned cases are 310.07 K, 308.91 K, 307.24 K, and 307.12 K, shown in figs. 10(a)-10(d). Therefore, it implies that novel materials with high thermal conductivity such as CNT and GNR may be potential materials for TTSV to address thermal problems in 3-D-IC in the future.

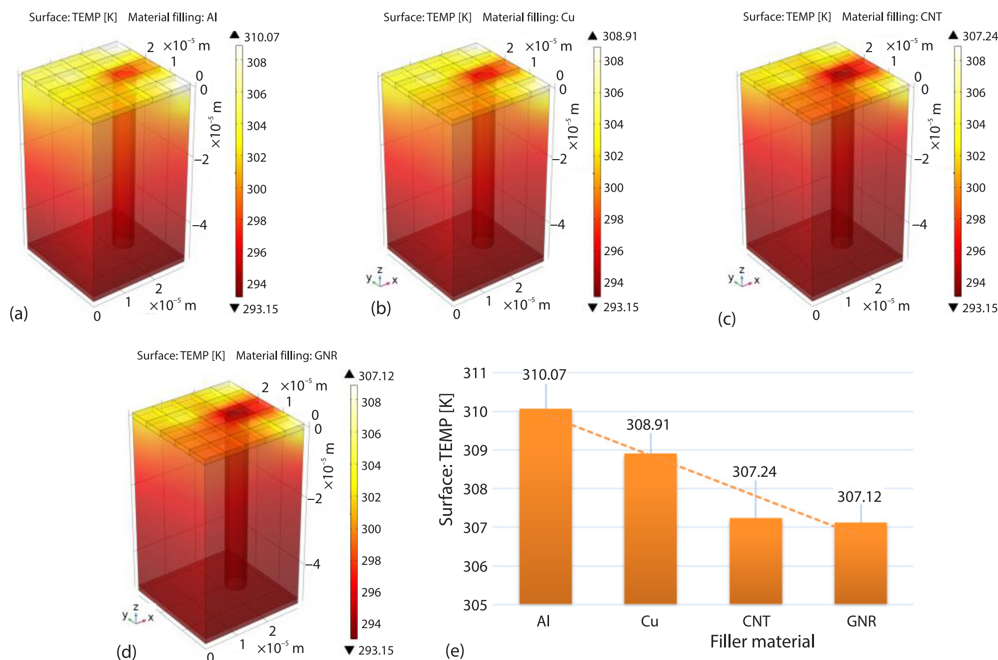


**Figure 10. Transient temperature fields in single-layer with various filler materials of TTSV at time $t$ = 1 second; (a) Al, (b) Cu, (c) CNT, (d) GNR, and (e) peak temperatures of all the cases mentioned previously**

## Conclusion

This paper reports a novel optimized method, which can effectively locate TTSV in non-uniform heat sources. Verification have been conducted on MATLAB software for 3-D-IC with single-layer and three-layer, respectively. In addition, the proposed method shows well agreement with COMSOL simulations. The results show that the optimized TTSV placement can significantly reduce the peak temperature of the chip. Meanwhile, the number and material of TTSV need further consideration during the thermal management of the 3-D-IC. Therefore, the optimized method is a promising method for solving complex thermal management in 3-D-IC.

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