AN ANALYTICAL THERMAL MODEL FOR THE 3-D INTEGRATED CIRCUIT WITH NEW-TYPE THROUGH SILICON VIA

by

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Through silicon via technology is a promising and preferred way to realize the reliable interconnection for 3-D integrated circuit (3-D IC), which can transfer heat from multiple dies to the heat sink in vertical direction. In this paper, a new general model of the through-silicon via (TSV) is proposed to investigate the thermal performance of the 3-D IC. The heat transfer characteristics of conical-annular TSV are studied for the first time. The impacts of different sidewall inclination angles and insulating layer thicknesses of TSV on the heat dissipation of 3-D IC were compared and analyzed in detail. As expected, our proposed model is in good agreement with the results of the existing models, which shows that the proposed model considering the lateral heat transfer and TSV structures can predict the distribution of temperature more efficiently and accurately. Furthermore, it is found that conical-annular TSV has more excellent heat dissipation performance.

Key words*: 3-D integrated circuit, analytical thermal model, lateral heat transfer, conical-annular TSV*

Introduction

Recently, the 3-D integrated circuits, integrating multiple device layers in the vertical direction, offers several advantages over its traditional 2-D partner in reducing its average wire length, wire delay, power consumption, footprint. However, it is difficult to realize effectively cooling as the power density of the chip increasing [1-5]. Establishing a micro-channel cooling is tough due to the smaller size of the chips. Obviously, thermal management has become the main factor determining the performance and reliability of 3-D IC [6-9]. Hence, it can be accepted that establishing an accurate thermal analysis model to predict the temperature of 3-D IC becomes extremely essential.

Vertical integrated circuits could reinvigorate Moore's Law that has slowed in recent years, which provides high density vertical interconnects [10, 11]. Heat dissipation is an important technology in 3-D IC. Temperature affects the operation performance of chips. The 3-D stack structure further increases the burden of heat dissipation. The TSV can be used for signal conduction but also for heat dissipation. Some scholars have used the heat dissipation TSV throughout the whole chip to achieve the purpose of heat dissipation. Therefore, it is necessary to conduct in-depth research on the heat dissipation film and TSV of 3-D IC.

There have been some achievements about the thermal analysis of 3-D IC with TSV. In Zhu *et al.* [12], a heat transfer model of 3-D IC was obtained considering TSV. However, it ignored the structures of TSV. In Qian *et al.* [13], the 1-D equivalent thermal model was

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established which overlooked lateral heat transfer. In Park *et al.* [14], the influence of height, diameter and shape of TSV were analyzed on the heat dissipation, but the effect of lateral heat transfer was unconsidered. The lateral thermal conductivity of TSV has a significant impact on the temperature profiles of 3-D IC [15]. In Liu *et al.* [16], the lateral thermal resistance of TSV was proposed considering physical and material parameters. In Ren *et al.* [17], an analytical model for the TSV unit cell was proposed, which demonstrated that simply using the vertical thermal conductivity of TSV for both lateral and vertical directions will overestimate its cooling performance in reducing the peak temperature. Therefore, it is necessary to build a model considering horizontal heat transfer and the structure of TSV. An equivalent thermal model for 3-D IC with the MLGNR-based TSV was proposed that took lateral heat transfer of through silicon via into account [18], but the model proposed in this paper only applies to rectangular TSV.

This study primarily aimed to investigate the thermal characters of 3-D IC with a new-type TSV. We build a model considering horizontal heat transfer and the structure of TSV. The following were the specific objectives of the study:

– to build architecture simplification model based on the cylindrical TSV, conical TSV, coaxial TSV and conical-coaxial TSV,
– to develop a 2-D thermal model of 3-D ICs with TSV,
– to compare and contrast the thermal characteristics of TSV under different architecture parameters, and
– to analyse heat transfer performance of TSV with four structures. To the best of the authors knowledge, the effect of multiple TSV on the heat dissipation of 3-D IC is investigated for the first time.

In addition, this model is more adaptable.

The new type TSV

As shown in fig. 1, various structures of TSV have been proposed include cylindrical, conical, coaxial and conical-annular. The TSV with different structures have different electro-thermal properties. The cylindrical TSV has a simple structure which is easy to model and analyze. The sidewall of the conical TSV with high reliability has a certain angle of inclination, which makes TSV compact and defect-free when filling the materials. The coaxial TSV with well signal integrity can reduce signal interference, transmission loss and delay [19]. Combining conical and annular to form a new-type TSV, which possesses both excellent performance [20].

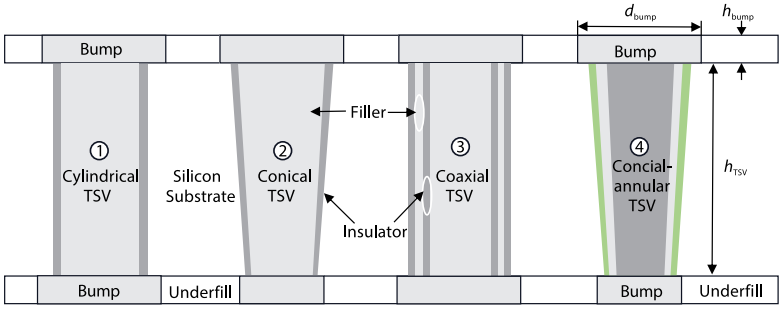

Figure 1. Cross-sectional view of TSV geometry

By analyzing the structural characteristics of different structures, we find common points for normalization. The materials composition of the conical and cylindrical TSV in the substrate are in the order of Si-Ins-Con. The conical-annular TSV structure consists of Si-Ins-Con-Ins-Si. Coaxial TSV structure is Si-Ins-Con-Ins-Con. Insulating layer is generally made

of SiO_2, Si_3N_4 or air. Filling materials (*e.g.*, Cu, Al, W, graphite and carbon nanotube) have high thermal conductivity. The insulating layer in the lateral direction plays a great impact on heat transfer with the difference in thickness and thermal conductivity [21].

For easier analysis, we normalize these structures to a simplification model as shown in fig. 2, the inner and outer layers are, respectively filling and insulating material. The R' and R are the outer and inner radius of the top insulation layer, respectively. The r' and r are outer and inner radius of the bottom insulation layer, respectively. The uniform thickness of the insulating layer is $\delta = R' - R = r' - r$. Where θ is the inclination angle of the side wall of the TSV and h is the height of TSV. The cone degenerates into a cylinder as $\theta = 90°$.

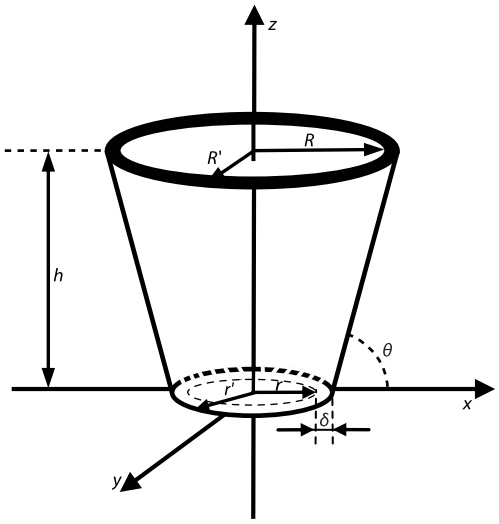

Figure 2. The TSV mathematical model

Thermal model of 3-D IC

As shown in fig. 3, there are two pathways for heat transfer. In the lateral direction, the main resistance comes from the conical insulating layer. Here, it is assumed that there is no contact thermal resistance. Where δ is the thickness of insulation layer and γ is the insulating layer cone radius. The conical surface area A is calculated according to the integral equation, which can be expressed:

$$\begin{aligned} A &= 2\pi\int_0^h (z\cot\theta + \gamma)\sqrt{1+\cot^2\theta}\,\mathrm{d}z \\ &= 2\pi\sqrt{1+\cot^2\theta}\left(\frac{\cot\theta}{2}z^2 + \gamma z\right) \\ &= 2\pi h\sqrt{1+\cot^2\theta}\left(\gamma + \frac{h}{2}\cot\theta\right), \quad r \le \gamma \le r',\ 0 \le \cot\theta \le \frac{R}{h} \end{aligned} \tag{1}$$

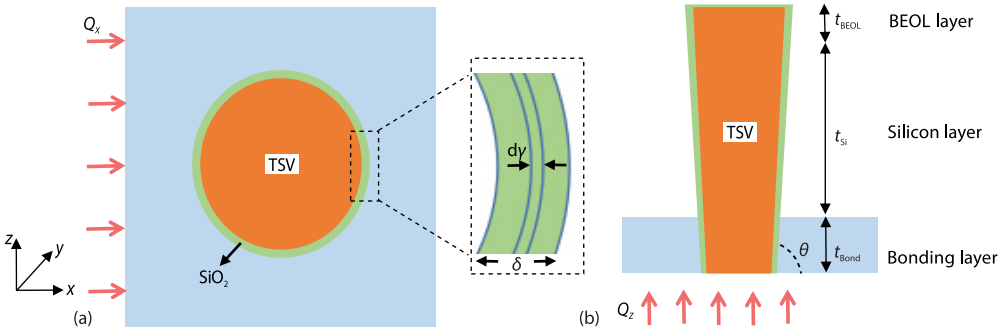

Figure 3. (a) Schematic of the *xy*-plane view of the TSV unit and (b) schematic of the *xz*-plane view of the TSV unit

The thermal resistance for TSV cell is similar to resistance in circuits, which can be defined as $R = t/Ak$, where t is thickness of material in vertical direction, A and k are cross-sectional area of material and thermal conductivity of material, respectively. Therefore, the R_{j1}, R_{j2}, and R_{j3} can be written:

$$R_{j1} = \frac{1}{S - \pi R'r'mn}\left(\frac{t_{\mathrm{Si}}}{k_{\mathrm{Si}}} + \frac{t_{\mathrm{Bond}}}{k_{\mathrm{Bond}}} + \frac{t_{\mathrm{BEOL}}}{k_{\mathrm{BEOL}}}\right), \left(j = 1, 2, ..., N\right) \tag{2}$$

$$R_{j2} = \frac{1}{mnk_{\mathrm{ins}}}\int_{r}^{r'}\frac{1}{A}\mathrm{d}\gamma, \ \left(j = 1, 2, ..., N\right) \tag{3}$$

$$R_{j3} = \frac{h}{\pi k_{\mathrm{con}} rRmn}, \ \left(j = 1, 2, ..., N\right) \tag{4}$$

According to the model of 3-D IC in fig. 4(a), we develop a 2-D thermal model of 3-D IC with TSV to represent the overall thermal model, and its equivalent thermal resistance model is shown in fig. 4(b). Here, R_{pk} and R_{hs} are thermal resistance of the package and heat sink, respectively. The T_{j1} is the temperature of j^{th} device layer. The T_{j2} represents the temperature of j^{th} TSV. The R_{j1} and R_{j3} represent the thermal resistance of the j^{th} die layer and the j^{th} TSV, respectively. The R_{j2} represents the lateral thermal resistance of the j^{th} isolation dielectric layer. The Q_j is the heat generated from the j^{th} device layer. The T_{amb} is the ambient temperature. The relationship between heat flow and temperature of the package, heat sink and other chip layers can be expressed from Kirchhoff's current law:

– For $j = 0$, we have:

$$\frac{T_0 - T_{\mathrm{amb}}}{R_{\mathrm{hs}}} = \frac{T_{11} - T_0}{R_{11}} + \frac{T_{12} - T_0}{R_{13}} \tag{5}$$

– For $j = 1$, we have:

$$Q_1 = \frac{T_{11} - T_{21}}{R_{21}} + \frac{T_{11} - T_{12}}{R_{12}} + \frac{T_{11} - T_0}{R_{11}} \tag{6}$$

$$\frac{T_{12} - T_0}{R_{13}} = \frac{T_{11} - T_{12}}{R_{12}} + \frac{T_{22} - T_{12}}{R_{23}} \tag{7}$$

– For $j = 2,...,N-1$, we have:

$$Q_j = \frac{T_{j1} - T_{j2}}{R_{j2}} + \frac{T_{j1} - T_{(j-1)1}}{R_{j1}} + \frac{T_{j1} - T_{(j+1)1}}{R_{(j+1)1}} \tag{8}$$

$$\frac{T_{j1} - T_{j2}}{R_{j2}} = \frac{T_{j2} - T_{(j+1)2}}{R_{(j+1)3}} + \frac{T_{j2} - T_{(j-1)2}}{R_{j3}} \tag{9}$$

– For $j = N$, we have:

$$Q_N = \frac{T_{N1} - T_{\mathrm{amb}}}{R_{pk}} + \frac{T_{N1} - T_{N2}}{R_{N2}} + \frac{T_{N1} - T_{(N-1)1}}{R_{N1}} \tag{10}$$

$$\frac{T_{N1} - T_{N2}}{R_{N2}} = \frac{T_{N2} - T_{(N-1)2}}{R_{N3}} \tag{11}$$

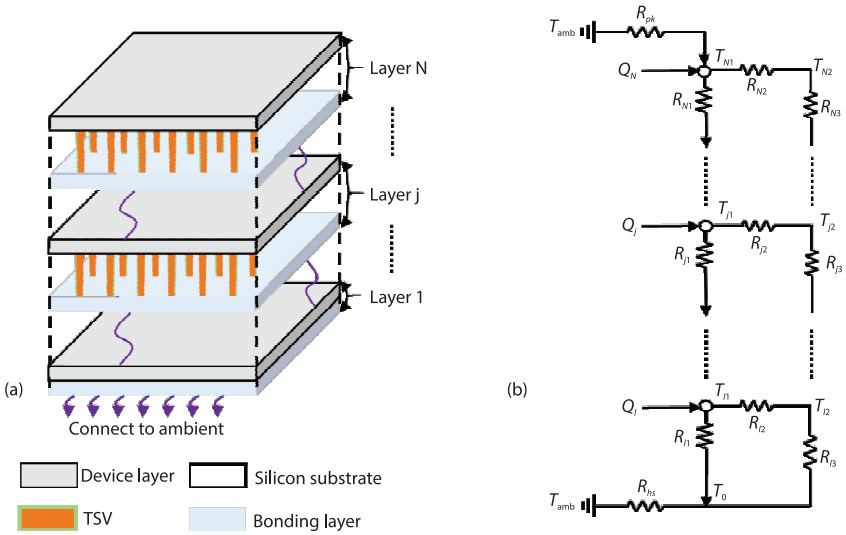

Figure 4. (a) A typical 3-D IC structure with TSV and (b) heat transport model considering lateral thermal resistance of TSV

The equivalent thermal resistance network model containing TSV can be obtained by eqs. (1)-(4), and the temperature of each layer [T_0, T_{11}, T_{21},..,T_{N1}, T_{12}, T_{22},..., T_{N2}] can be obtained by combining eqs. (5)-(11) with a total of $2N + 1$ equations.

Results and discussion

For the convenience of analysis, it is assumed that the device layer, silicon substrate and bonding layer of all dies have the same geometric structure and each device layer generates the identical heat, especially $R_{11} = R_{21} = R_{N1}$, $R_{12} = R_{22} = R_{N2}$, $R_{13} = R_{23} = R_{N3}$, $Q_1 = Q_2 = Q_N$. Furthermore, ambient temperature T_{amb} is set to be 25 °C. The overall package and heat sink thermal resistances are defined as $R_{pk} = 20$ K/W, $R_{hs} = 3$ K/W. The overall chip area is $S = 20$ mm × 20 mm. The thickness of silicon substrate, bonding layer, and BEOL layer are listed as follows, $t_{Si} = 60$ μm, $t_{Bond} = 5$ μm, $t_{BEOL} = 60$ μm. The heat generate of each layer is defined as 5.6 W. Temperature rise can be expressed as $\Delta T = T_i - T_{amb}$.

Trend of ΔT with angle θ and chip layers i

In Wang *et al.* [20], a small amount of TSV insertion was verified to reduce the peak temperature and inter layer temperature gradient. With the further increase of TSV density, the heat dissipation capacity of TSV on temperature rise tends to be saturated. Temperature rise with carbon nanotubes and graphene materials is significantly lower than that using Cu and W as filling materials. In this paper, Cu (400 W/mK) is used as the filling medium, $\rho_{TSV} = 5\%$ is the density of TSV that saturated, $m = n = 10$, a single TSV radius $R' = 250$ μm. Assuming that the thickness of the insulating

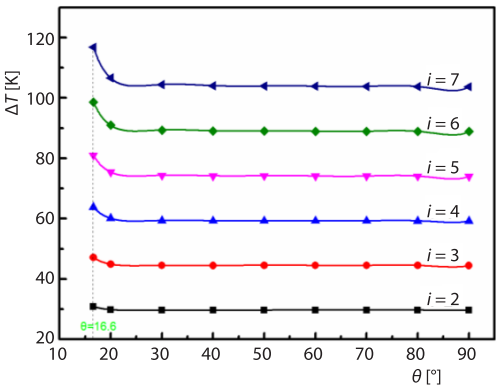

Figure 5. Trend of chip temperature rise with angle θ and layers i

layer is $\delta = 2$ μm. The chip temperature rise and the TSV sidewall inclination are shown in fig. 5. As is shown in tab. 1, for the sidewall inclination angle decreases to about 20°, the temperature rises faster. It becomes aggravated as the number of chip layers increasing.

Table 1. Chip temperature rise, ΔT [K], with angle θ and layers i

i	θ								
	90°	80°	70°	60°	50°	40°	30°	20°	16.6°
2	29.702	29.709	29.715	29.718	29.724	29.73	29.738	29.837	30.853
3	44.458	44.468	44.47	44.478	44.543	44.564	44.64	44.898	47.14
4	59.245	59.263	59.271	59.275	59.29	59.29	59.371	60.085	63.834
5	74.033	74.059	74.077	74.095	74.193	74.162	74.319	75.431	81.005
6	88.851	88.879	88.91	88.945	89.047	89.076	89.326	90.948	98.643
7	103.71	103.728	103.797	103.845	103.903	104.037	104.39	106.604	116.775

Impact of insulation layer thickness δ and thermal conductivity k on ΔT

Assuming that the number of chip layers is 6, the TSV sidewall inclination angle is 60°. The effect of thickness of the insulating layer on the chip temperature is shown in fig. 6. The heat transfer resistance in the lateral direction enlarges with the increase of the insulating layer. The 1-D thermal resistance model with TSV ignored the effect of lateral heat transfer. In this work, insulation material is SiO_2. With the increase of thermal conductivity, its impact on temperature tends to be saturated. If these factors are excepted, the error of the temperature value will increase. Graphene has extremely high thermal conductivity as high as 5300 W/mK, which is much larger than that of traditional metal heat dissipation materials Cu and Al [22]. High thermal conductivity and other excellent properties make graphene becoming the next-generation heat dissipation and thermal management material. Materials with high thermal conductivity can greatly improve the lateral heat transfer capability. As is shown in tab. 2, it can be observed that the steady-state temperature rise of low thermal conductivity is higher than others.

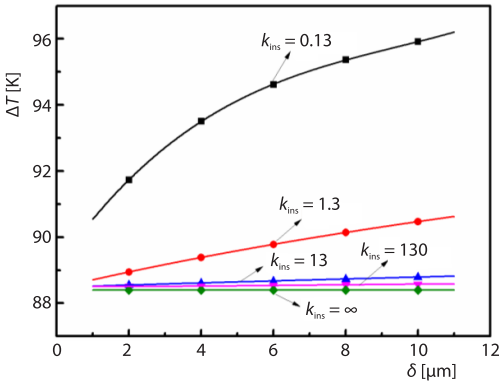

Figure 6. Insulation layer thickness δ and thermal conductivity k on ΔT

Table 2. Chip temperature rise, ΔT [K], with insulator thickness δ and thermal conductivity k

δ [Wm^{-1}K^{-1}]	k_{ins}				
	2 μm	4 μm	6 μm	8 μm	10 μm
0.13	91.73	93.507	94.613	95.366	95.912
1.3	88.945	89.384	89.78	90.139	90.468
13	88.548	88.612	88.672	88.732	88.79
130	88.507	88.518	88.532	88.557	88.575
∞	88.401	88.401	88.406	88.410	88.417

Thermal analysis for different TSV geometries

Based on the aforementioned discussions, we investigate the thermal transmission differences among different TSV structures. As shown in fig. 7, ①②③④ represent different structures shown in fig. 1, respectively. It is obvious that the temperature rise will be increased with the rising of chip layers. Each geometry has different thermal transmission performances. In addition, under the same conditions, we can conclude that ③ and ④ not only have more excellent electromagnetic properties, but have better thermal conductivity than ① and ②. Generally, ④ > ③ > ② > ①.

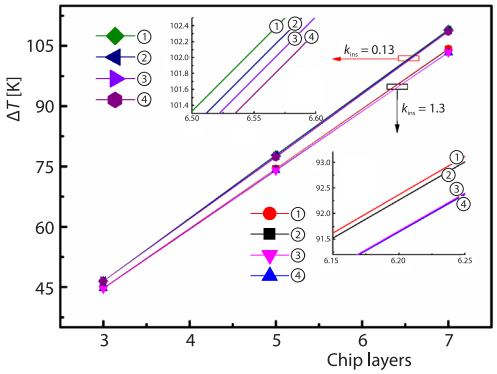

Figure 7. Thermal analysis for different TSV geometries

Conclusions

The paper presents a new general model of the TSV which is suitable for a variety of TSV structures. Then we establish a new analytical thermal model considering the lateral heat transfer. On the basis of the previous analysis, the following design guidelines can be concluded, are as follows.

- The inclination angle of TSV should not be low, or the heat dissipation performance will be seriously reduced.
- Insulation layer should be selected with high temperature coefficient materials and appropriate thickness for the excellent heat dissipation.
- Results show that conical-annular TSV can reduce the chip temperature more effectively compared with other TSV. Therefore, the conical-annular TSV as a new emerging TSV has a better application prospect in the 3-D IC. Consequently, the heat transfer characteristics of conical-annular TSV are studied for the first time. The proposed thermal model in this paper is expected to study the thermal characteristics of TSV array in the future.

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Nomenclature

k – coefficient of thermal conductivity, [Wm^{-1}K–1]
Q – heat flow, [W]
R – thermal resistance, [KW^{-1}]
T – temperature, [K]

Greek symbols

δ – thickness of insulation layer, [μm]
γ – insulating layer cone radius, [μm]
θ – the inclination of the side wall of the TSV, [°]

Subscripts

amb – ambient
BEOL – back-end interconnect layer
Bond – bonding layer
con – conductor
hs – heat sink
ins – insulator
pk – package

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