COOLING ENHANCEMENT OF CUBICAL SHAPES ELECTRONIC COMPONENTS ARRAY INCLUDING DUMMY ELEMENTS INSIDE A RECTANGULAR DUCT

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Abstract

In this work, numerical simulation has been done to study the cooling enhancement of electronic components of cubical shapes including dummy elements inside a rectangular duct. 12 electronic chips (3 x 4 array) of dimensions (50 mm x 50 mm x 10 mm) are tested in an air duct of dimensions (350 mm x 3500 mm x 60 mm). The aim of the simulation is to study the influence of changing positions of the hot components on the overall cooling performance at different Reynolds numbers. Moreover, the effect of spacing between electronic components is studied. This is achieved by changing the position of the heat sources while keeping other elements as dummies to keep the flow characteristics. The Reynolds number is in the range (500 to 19000). The standard k-ε, model is used and validated with experimental work showing *good agreement. 37 cases per Reynolds are considered, resulting in an overall 259 studied cases. It is concluded in terms of the large resulting data from this study that, increasing the spacing between elements in the cooling fluid flow direction influences the cooling rate. Moreover, designers should be interested to operate such systems at optimized higher Reynolds values.*

Keywords: *Heat transfer, electronic device cooling, Heat Source, Dummy, Numerical*

1. Introduction

The cooling process of electronic devices such as cellular phones, notebooks, laptops, digital cameras, control systems in missiles, and battery modules of electric vehicles, becomes challenging. Because of, the enhanced design of processing speed and miniaturization of the size of such devices. Which causes a higher heat generation and consequently increases the operating temperature to a dangerous value beyond the critical limits. Since the failure rate of these devices is directly related to the operating temperature, it is important to enhance the cooling process. Many researchers have been attracted to this area of research by suggesting and developing new techniques for the cooling process of electronic devices Refaey et al. [1] and Ali et al. [2]. Generally, the development of cooling for thermal heating sources takes several directions like the material of elements (enhance thermal conductivity [3]), using phase change materials (PCM) [4], structure design (use of pin-fins [5 and 6]), spacing, flow rates of cooling fluids, etc. In addition, Bahiraei and Heshmatian [7] introduced a review of utilizing nanofluid as a novel coolant with minichannel to miniaturization of electronic components. Bahiraei and Monavari [8] examined the effect of nanoparticles of different shapes in a microchannels heat sink with various Reynolds numbers. The outcomes revealed that the suspension with platelet particles had the lowest thermal resistance.

The focus of the present paper is on studying the influence of spacing between heat sources as well as the cooling fluid flow rate on the cooling process of a circuit board of an electronic device. Greiner [9] demonstrated that the convective heat transfer was reduced due to slow recirculation in channeled areas and diffusion is the main mechanism that transferred heat. Alam et al. [10] presented a numerical study to cool a heat sink of triangular pins. The results denoted that the Nusselt number (Nu) increases by increasing the velocity of airflow which enhanced the heat extraction from the CPU. Ali et al. [11] compared experimental and numerical data for the effect of spacing among two-element heat sources. They presented correlations for Nusselt number as a function of Re within a range of $2464\ 6 \leq Re_L \leq 16{,}430$ and package spacing ($1 \leq S \leq 3$). Farhanieh et al. [12] presented the characteristics of heat transfer in grooved channels. The results showed that there was a big influence of the flow reattachment and recirculation on the heat transfer rate from heated elements. The results showed that there was about a 300% increase in the heat transfer when comparing grooved channels results with flat channel flow. The laminar and turbulent flows with a local heat flux for a heated array block were simulated by Asako and Faghri [13]. The results showed that the transportation was larger from the upper surface compared to vertical sides in dense arrays.

Molki and Fagri [14] presented the forced convection of in-line rectangular blocks cooled by air. Nakayama and Park [15] studied analytically and experimentally the conjugate heat transfer from a rectangular block mounted in an airflow. Kurşun and Sivrioğlu [16] investigated numerically the effect of the U-shaped flow routing plate on laminar mixed convection heat transfer in a rectangular channel. An enhancement of (180%) was observed in the study. Bahiraei et al. [17] performed a numerical study on the elliptical pin-fin heat sink. Silver–water nanofluid was used to enhance the cooling and gave an appreciable positive effect. The findings showed that there was a maximum boost in the heat transfer coefficient of 49.6% as the fin density increased. Furthermore, Bahiraei and Mazaheri [18] examined the performance of spiral liquid blocks to cool the electronic processors with graphene nanoplatelets. The outcomes proved that the spiral liquid block allowed exceptional heat transfer which is recommended from the energy efficiency perspective.

Refaey et al. [1] performed a numerical and experimental study for heat transfer enhancement of cubical heat sources (12 elements) inside a rectangular duct. The research focused on the influence of both spacing between elements and cooling air flow rate on the heat transfer characteristics. Where the work; CFD, experimental considered only two heat source elements and the rest are dummy elements just to keep the flow characteristics. For a Reynolds number range of $4108 \leq Re_L \leq 17{,}115$. The experimental results showed that the farthest the second heat source gives the highest heat enhancement of the first upstream heat source with an enhancement ratio of 17% and 10% at $Re_L = 8538$ for in-line and lateral locations, respectively. The numerical results demonstrated that when all elements in the array are heated and compared with two heat elements only, a maximum reduction of about 19%, 15% in average Nusselt number for, an in-line and lateral position obtained when the second heat element is located at position 8 and 4, respectively at Re =17,115. Their work implied that a lot of cases needed to be studied to get a detailed conclusion on such a topic.

Hence, the present work aims to present a numerical CFD simulation with a wide range of Reynolds number. Because executing the experimental works with the test rig presented by Refaey et al. [1] was very difficult with low ranges of Reynolds number. Therefore, a numerical CFD simulation is the best way to represent such investigations. So, expanding the range of Reynolds number, low range, and higher range, Re from 500 to 19000 was studied. Then, a huge number of cases regarding the heat source positions formed 259 cases were studied in the present work. This huge number of CFD cases provided the ability to study the influence of changing positions of the hot components on the electronic board. In addition, the overall cooling performance at a wide range of Re numbers and the effect of spacing between electronic components (heat source elements) is investigated.

2. Numerical analysis

2.1 Computational domain

The computational domain is designed to simulate the flow of cooling air through or over an array of rectangular blocks representing electronic components (heat sources or chips 3x4) that are attached to a circuit board. The aim of the simulation is to study the influence of changing positions of the hot components on the overall cooling performance at different Re numbers, other means studying the effect of spacing between electronic components. Changing positions strategy has been built on the followings: all components with heat (on), only one component (any one of them by order) without heat which is then considered as a dummy element just to keep the flow characteristics, two or more components without heat in the same inline, lateral or other defined planes. Forming different 37 cases per each studied Re number value (seven points) with a total number of 259 cases to be studied.

2.2 Geometry

A 3-dimensional geometrical model is designed using ANSYS-Design Modeler R18.0 as shown in Fig. (1). Figure (2) describes full details of the experimental test rig and test section details used in the computational domain. The chips domains are an array of twelve rectangular aluminum blocks (3 columns x 4 rows). The first chips row is positioned at 500 mm from the duct entrance to assure fully developed flow conditions and lies at the bottom of the duct. The full description of the test rig was demonstrated by Refaey et al. [1].

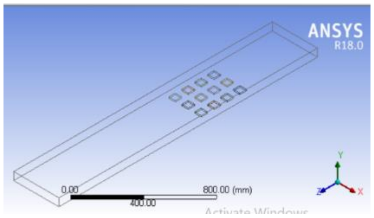


Fig.1: Computational domain

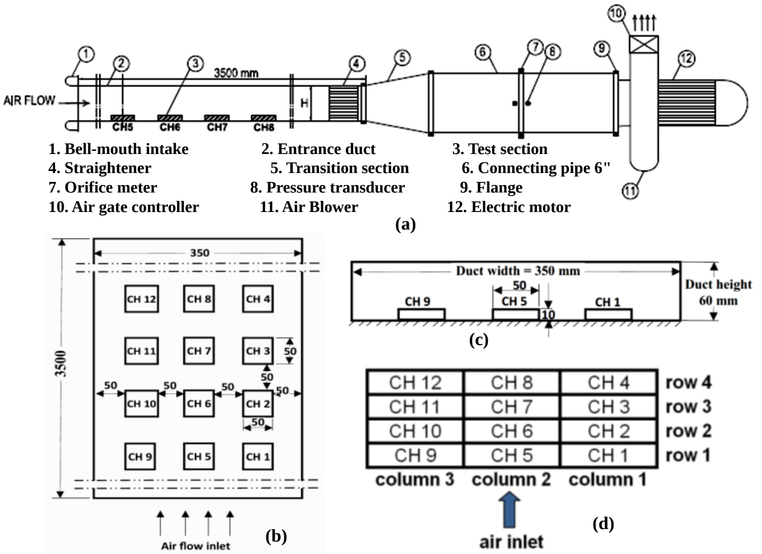


Fig. 2: Experimental test rig used by Refaey et al. [1]; (a) details view (b) top view of test section (c) sectional view (d) columns and rows arrangement

2.3 Equations

In the following sections, some calculated parameters will be represented. Therefore, they should be predefined at first. The heat flux, q, and the average heat transfer coefficient are calculated as follows in Eqs. (1), and (2) [11], respectively:

$$q = \frac{\mathrm{Q_{net}}}{A_s} \tag{1}$$

$$h = \frac{\mathrm{q}}{T_m - T_{ai}} \tag{2}$$

The Reynolds, $\mathrm{Re_L}$, and average Nusselt, $\mathrm{Nu_L}$, numbers are defined based on the chip length in fluid flow direction as follows [11]:

$$\mathrm{Re}_L = \frac{\mathrm{v\ L}}{\upsilon_a} \tag{3}$$

$$Nu_L = \frac{\mathrm{h\ L}}{k_a} \tag{4}$$

2.4 Mesh generation, model selection, boundary conditions, and solution method

A 3-dimensional uniform volume mesh is generated in the computational domain. The mesh is created using the tetrahedron elements for the air domain and structured elements for the chips domains. The effect of the boundary layer developed over the chips walls on the CFD results is resolved by generating a very fine mesh near the chips walls with the dimensionless y + maximum value of 1.0. The fine mesh near the walls consists of 18 layers with a first-layer thickness of 0.08 mm at an inflation rate of 1.2. The boundary conditions are as follows: fluid inlet velocity at the inlet according to ReL value range from 500 to 19000, including seven points; 500, 1000, 1500, 5000, 9000, 13000, and 19000, the inlet temperature is 300 K, pressure outlet is used at the fluid outlet, adiabatic air duct walls, and adiabatic chips bottom walls. The heat generation of all heat sources taken is 140000 W/m^3 (3.5 W). Several models were examined and the standard κ – ε model is used for the turbulence model with a turbulence intensity of 5 % as verified by Refaey et al., [1] as shown in figure (3). The governing equations: continuity, momentum, and energy equations (Eqs. (5), (6), and (7)) for temperature distribution, flow field, and heat transfer in the duct are applied and solved in the Cartesian coordinate system as represented by Ali et al. [11]. The solution of the present model is converged when continuity, momentum, and energy residuals reached 10^{-4}, 10^{-6}, and 10^{-7}. A mesh independence test is performed using different five sets of grids. Based on a criterion, of calculating the average surface temperature of chips 5, 6, 7, and 8 at Re value of 5000. Table 1 tabulates the grid test study and shows that the increase in cell counts above 558,128 leads to a marginal change in temperatures, so it is used for all the studied cases in the present work.

$$\nabla.(\rho U) = 0 \tag{5}$$

$$\nabla.(\rho UU) = -\nabla P + \nabla.[\mu_t(\nabla U + \nabla U^T)] \tag{6}$$

$$\nabla.\left(-\mathrm{k}\nabla \mathrm{T} + \rho C_p T U\right) = S_h \tag{7}$$

Where, S_h is the thermal source term.

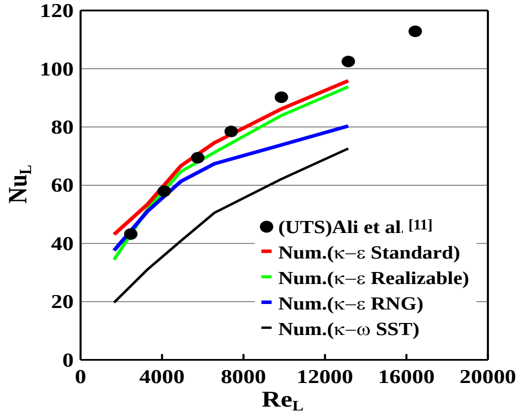


Figure (3): Model selection and comparison with Ali et al. [11].

Table 1: Mesh independency study (Re 5000 – all chips are heat sources)

	Total number of nodes/cells	Chips' average surface temperature [K]			
		Ch 5	Ch 6	Ch 7	Ch 8
Grid 1	100,545 / 320,805	322.025	328.289	330.658	331.520
Grid 2	118,514 / 413,187	321.751	327.263	329.810	331.441
Grid 3	149,461 / 558,128	323.711	329.158	331.954	333.140
Grid 4	188,650 / 771,436	323.851	329.142	331.656	332.961
Grid 5	220,853 / 931,553	323.782	329.310	331.693	333.102

2.5 Model validation

The numerical model is validated using the experimental results for the Reynolds range between 3611 and 14174 presented by Refaey et al. [1]. Where, the experimental test section represents a flow of air in a rectangular duct with the same dimensions and with the same chip's array (3x4) in the current model. While the experimental work of Refaey et al. [1] considers heat energy for one chip in position 5 (as a single heat source - SHS) or two heat sources in both positions 5 and 6. Figure (4) illustrates the validation of the present numerical model and showed a good agreement between the numerical and the experimental results with an average deviation of 14.6%.

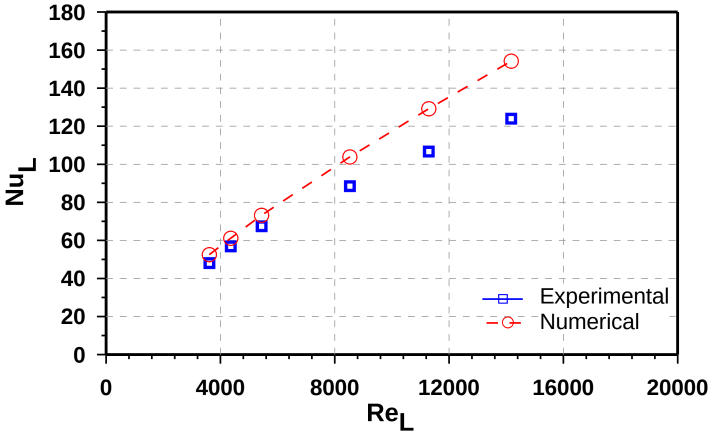


Figure (4): Model validation with experimental work of Refaey et al. [1].

3. Results and Discussions

Since there are many results (259 simulations) in the present study, it is difficult to represent all these results directly. So, it is planned to show samples from the results that perfectly served the concluded remarks from this study.

3.1 All chips are heat sources

Figure (5) represents the results when all chips are considered as heat sources. Figure (5-a) gives the temperature contours at two Reynolds numbers; 500 and 19000. The figure represents three views: chips only, chips and airflow, and a side view of airflow direction. From Fig. (5-a) it could be deduced that for higher Re_L the temperatures of the chip area are reduced and an average of 34% decrease in the temperature can be reported for Re_L =19000 when compared to Re_L 500. This is mainly due to the increase in the cooling rate because the air velocity effects to increase in the convection coefficient. Also, it is noticed that the farthest elements from the duct inlets attained the highest values of temperatures. Consequently, poor cooling rate at these elements. Same remarks can be drawn from Figs. (5-b) and (5-c) which demonstrates that, the influence of Re_L on the resulted temperature is much larger when $Re_L < 5000$, while lower influence is reported for $5000 < Re_L < 10000$, and a marginal influence attained at $Re_L > 10000$. For example, the temperature of chip 1 drops by an average 22.4% in the range of $Re_L < 5000$, by 4.2% in the range ($5000 < Re_L < 10000$), and by 0.64% in the range $Re_L > 10000$. This can be attributed to the change in the flow behavior from laminar to turbulent based on Re_L where the turbulent flow is characterized by enhanced heat transfer characteristics. Moreover, the 4th row reports a poor average Nu_L of about 26.6% than the first row.

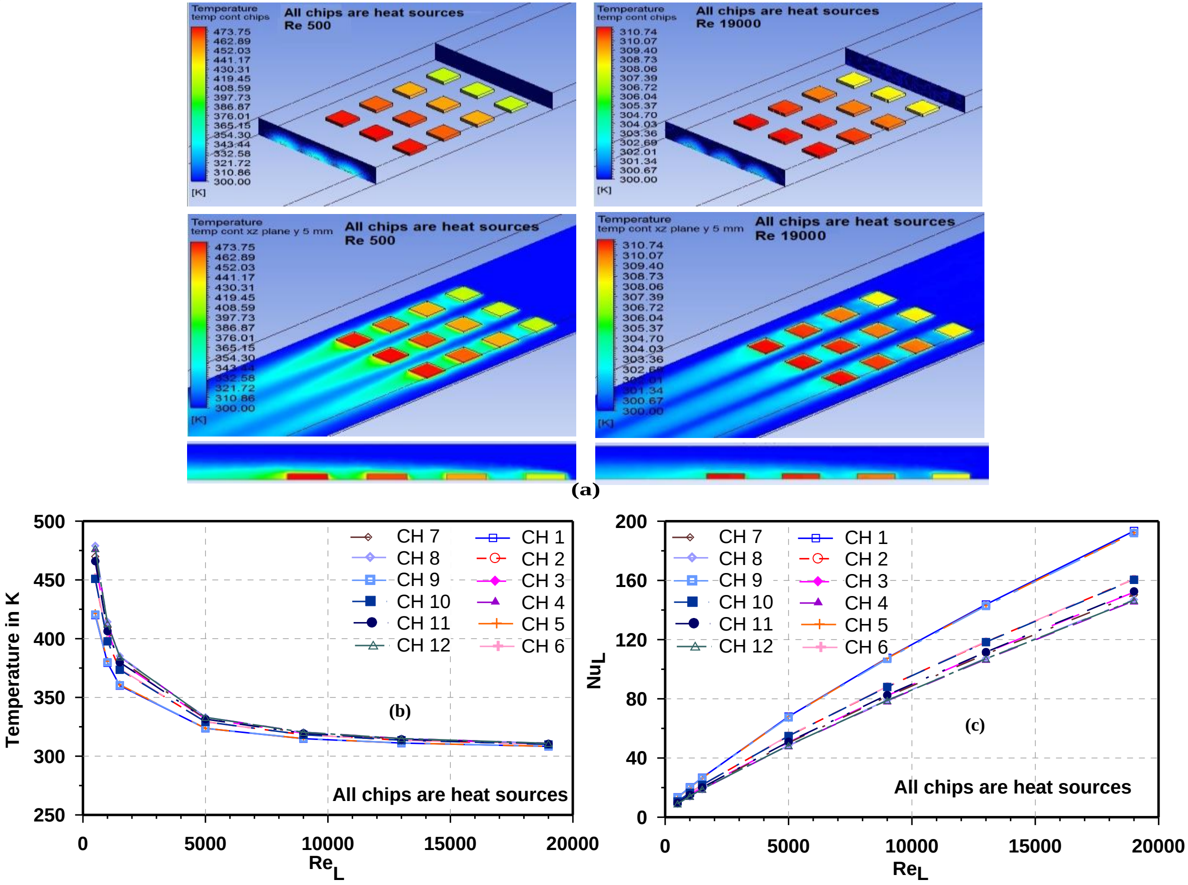
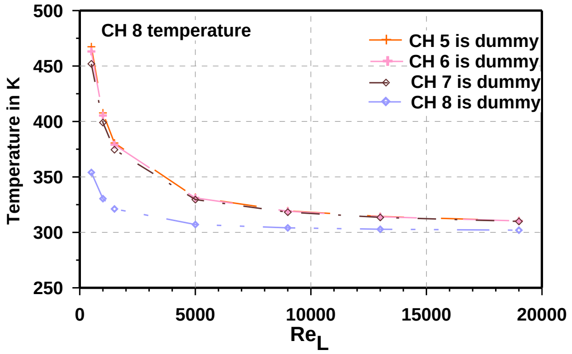


Figure (5): Variation of temperature and Nusselt number for the case, all chips are heat sources (a) Temperature contours (b) chips temperatures with Re_L, (c) chips Nu_L with Re_L.

3.2 One chip is a dummy element

Figure (6) represents the variation of chip 8 temperature when one chip is a dummy in its column (column 2) and the others are heat sources. It could be drawn that, moving on the position of the dummy element in the same column, from chip 5 toward chip 8, results in a decrease in chip 8 temperature at the same Reynolds number. For example, chip 8 temperature at Re_L 5000 attained a temperature of 331.57 K when chip 5 is a dummy and 307.1 K when chip 8 itself is a dummy. This is mainly due to the increase in the space between the target chip (chip 8) and the previous heat source which affects the cooling rate. In other words, chip 8 attained its maximum temperatures for all Reynolds number when the dummy element is far from it. This means that, for much cooling rate, there should be a distance between the two perspective chips.



Figures (6) Variation of chip 8 temperature with Re_L at different dummy chips (in columns 2).

3.3 Two chips are dummy elements

Figure (7) shows a sample of the results when two chips are dummy, and all other chips are heat sources. It illustrates the variation of chip temperatures (in column 1) with Re_L. It could be concluded that the temperatures of chips 1 and 2 are almost the same and constant along with Re_L because they are at the beginning of the same column. Also, it is observed that the temperature values of chip 4 are higher than that of chip 3. The figure as the flow inlet velocity rises the side combination among the airflow and recirculation flow enhances. Moreover, the two heat source temperatures decrease as inlet flow velocity increases. This is due to flow impingement on the second dummy element (chip 2) at superior inlet velocity as shown in figure (7).

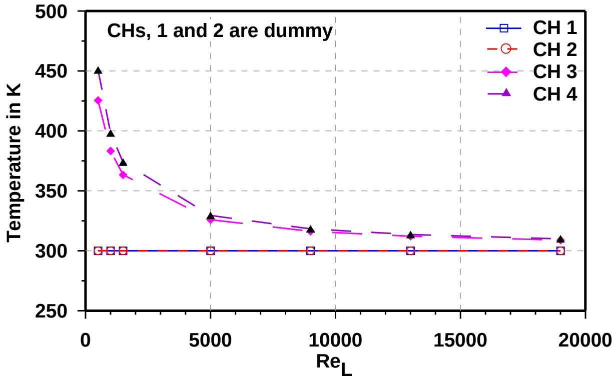


Figure (7): Sample case of two chips is the dummy (chips 1, 2) and the rest chips are heat sources.

3.4 One row or two rows and or one column is a dummy

Figure (8) represents the results for the case of one row and two rows being the dummy, and all other chips being heat sources. The figure illustrates the variation of all chips temperatures with Re_L. It could be drawn from Fig. (8) that, the results, in this case, could be accounted for and analyzed for each row as a whole body. It is worth noting from Fig. (8-a) that, row 4 attained an average temperature of 331.9 K while row 2 attained 325.75 K at Re_L 5000 by an increase of 1.85% which indicate a decrease in Nu_L of 18.5%. Figure (8-b) the variation of all chips temperatures with Re_L when row 1 and row 3 are dummies at the same time. It is noticed that the temperatures of the last row (row 4) are decreased due to the small heat gained from the flowing air because row 3 is a dummy. In addition, as the flow inlet velocity rises the side combination among the airflow and recirculation flow enhances after the first row. Moreover, the last row temperatures increase due to it being a source term and the flow coming from previous rows carrying heat and releasing a low amount of heat from it. This is mainly due to the increase in the space between the chips in the last row and the previous heat source (due to making row 3 a dummy) which affects the cooling rate.

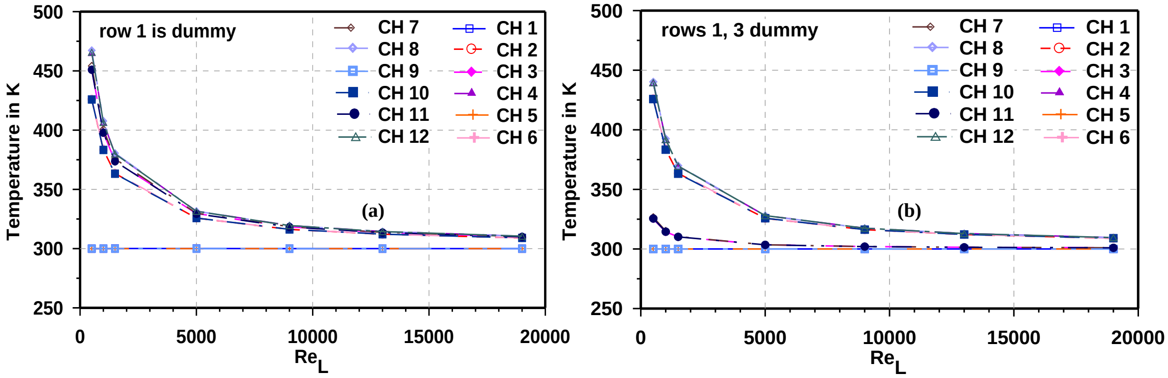


Figure (8): Variation of chips temperature against Re_L (a) Row 1 is dummy (b) Row 1, and 3 are dummies.

Figure (9) illustrates the variation of all chips temperatures with Re_L when column 2 is a dummy. It is worth noting that, column 2 is positioned at the centerline of the domain, hence, there would be an asymmetry between column 1 and column 3. It could be drawn from Fig. (9-a) that, chips on the right-hand side from column 2 attained the same temperature and consequently Nusselt number as the chip on the left-hand side. Therefore, it is not useful to switch the elements in the same column because it does not affect the cooling rate of such an electronic circuit.

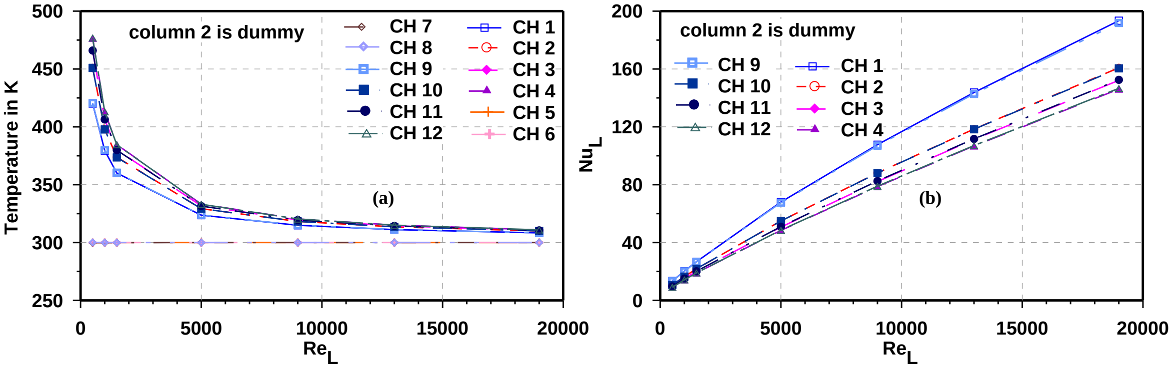


Figure (9): Case of one column is dummy (a) Variation of chips temperatures (b) Variation of Nu_L.

3.5 Influence of spacing and cooling fluid flow rate on the max. & min. overall average chips temperatures

It is important to get general concluding remarks based on the large results of this study that can be helpful for the designers in this field. This remark should answer the interesting question: which arrangement is better for increasing the cooling rate? So, it is planned to calculate the overall average temperature of all chips in all cases for each studied Re_L. The results are illustrated in Fig. (10) and showed that for all studied Re_L values the maximum overall average chips temperature is reported for the case all chips are heat sources, which makes sense. While the minimum overall average chips temperature which represents the enhanced cooling is reported for the case of two rows 1, 3 are dummy and the rest are heat sources. Therefore, increasing the spacing between elements in the cooling fluid flow direction influences the cooling rate. Also, the results assure that the difference between the maximum and minimum overall average chips temperatures is large at lower Re_L (< 5000) and marginal at higher ReL. This is mainly due to the heat transfer characteristics enhancement along with the increase in Re_L. The difference found to be 81.3 K at Re_L 500, 15.1 K at Re_L 5000, 9.3 K at Re_L 9000, 6.9 K at Re_L 13000 and 5.1 K at Re_L 19000. Indicating that, designers should be interested to operate such systems at optimized higher Re_L value to fill in the circuit with the maximum needed number of chips.

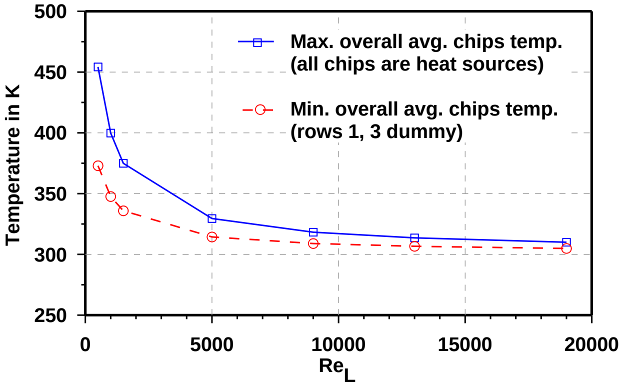


Figure (10): Influence of the cooling fluid flow rate (Re_L) on the maximum and minimum overall average chips temperatures.

4. Conclusions

This paper represents a large numerical simulation that has been done to study the cooling enhancement of electronics components of cubical shapes including dummy elements inside a rectangular duct. 12 electronic chips (3 x 4 array) are tested in an air duct with a wide range of Re_L; 500 to 19000. The work is focused on studying the influence of change both, spacing between chips, and cooling airflow rate, on the cooling enhancement. This is attained by changing the position of the heat sources while keeping other elements as dummies just to keep the flow characteristics and the following points are withdrawn:

- Increasing the inlet flow rate decreases the chips' temperatures.

-The influence of Re_L on the resulted temperature is much larger when $Re_L < 5000$, lower influence reported for ($5000 < Re_L < 10000$), and with marginal influence for $Re_L > 10000$.

-The farthest elements from the duct inlets attained the highest values of temperatures.

- Increasing the spacing between elements in the fluid flow direction, influences the cooling rate.

- Designers should operate such systems of an electronic board at optimized higher Re_L values.

- The maximum overall average chips temperature is reported when all chips are heat sources.

- The minimum overall average chips temperature which enhances cooling is obtained when rows 1, and 3 are dummies and the rest are heat sources.

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Nomenclature

As: heat element surface area, [m^2]
h: convection heat transfer coefficient, [$W/m^2.K$]
k: thermal conductivity, [W/m.K]
L: heat source length, [m]
Q: heat transfer rate, [W]
q: heat flux, [W/m^2]
T: temperature, [K]
v: mean velocity, [m/s]
L: based on chip length
m: mean
net: net amount of heat

Dimensionless groups

Nu: average Nusselt number
Re: Reynolds number

Abbreviations

avg: average
CFD: Computational Fluid Dynamics
CH: chip
CPU: Central processing unit

max: maximum
min: minimum
PCM: phase change material
RANS: Reynolds Averaged Navier-Stokes
SHS: single heat source
temp: temperature

Greek letters

ν: kinematic viscosity, [m^2/s]

Subscripts

1:12: chips numbers
a: air
i: inlet

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