INVESTIGATION ON THE HEAT DISSIPATION OF HIGH HEAT FLUX CHIP ARRAY BY FRACTAL MICROCHANNEL NETWORKS

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With the development of integrated circuits, high power and high integration chip array devices are facing the requirements of high heat flux and temperature uniformity. The microchannel heat sink can meet the heat dissipation requirements of chip array devices with high heat flux, and the flow channel with fractal structure can achieve high temperature uniformity of chip array. In this study, the H-shaped fractal microchannel structure was proposed to cooling the 4×4 chip (1 × 1 mm) array. The interior fillet structure (IFS) was introduced to optimize T-shaped and L-shaped corner structures in the fractal channel. The simulation results show that the overall pressure drop of microchannel heat sink with IFS is reduced 18.7%, and the maximum temperature difference of 4×4 chip array is less than 1.2 ℃ at 1000 W/cm². The microchannel heat sink with IFS was fabricated and assembled, and the hydro-thermal performance was characterized by thermal test chip (TTC) at different flow rates and heat fluxes. The experimental results show that the standard deviation of temperature of 4×4 chip array is less than 3.5 ℃ at 1000 W/cm² and 480 ml/min. The error between experimental and simulation data is within ±1.5%, which proves the reasonability of computational fluid dynamic (CFD) modeling and simulation. And furthermore, the results demonstrate that by introducing IFS into the T-shaped and L-shaped structures could reduce pumping power and improve temperature uniformity of chip array, which can be applied to improve the performance of the chip array devices with high heat flux.

Key words: chip array, TTC, fractal microchannel, temperature uniformity

1. Introduction

With the development trend of high power and performance of chip array in microsystem, the size of chip array is gradually becoming miniaturized and multi-integration, which brings increasing challenges to the thermal management of chip array. Taking the T/R (Transmitter and Receiver) component array for example, the heat flux of the next-generation of active phased array radar exceeds 1000 W/cm² [1]. A low temperature gradient of the T/R component array (less than 10 ℃) is required [2], because the temperature gradient will lead to the phase deviation of the output signal, which will
affect the beam space synthesis of the antenna. Therefore, it is necessary to improve the temperature uniformity while cooling the chip array with high heat flux.

Traditional cooling technologies such as natural convection and contact-type heat conduction cannot achieve effective heat dissipation of high heat flux chip [3]. Microchannel heat sink has a large heat transfer area and coefficient [4], which can achieve heat dissipation for chip with 710 W/cm² [5]. However, the temperature rise of the coolant along the flow direction in the traditional straight microchannel will affect the temperature uniformity of the chip [6]. The method to improve the temperature uniformity of chip is to increase the convective heat transfer coefficient or heat exchange area of the microchannel heat sink to reduce the temperature rise of coolant along the flow path [7]. For example, wavy microchannel [8], gradient distribution pin fin [9], variable-height microchannel [10], microchannel with cavities and extended surface [11], offset zigzag microchannel [12] are used to improve the convective heat transfer coefficient and heat exchange area. The double-layer microchannel [13,14] is used to reduce the temperature rise of coolant along the flow path.

Constructal-theory network [15] is an effective method to improve coolant flow uniformity and temperature uniformity of chip array. The fractal channel network structure has higher temperature uniformity [16], higher heat dissipation efficiency [17,18], and lower thermal resistance [19]. Wei and Huang [20] studied the multi-layer silicon microchannel cooler for 4×4 chip array with H-shaped bifurcation structure. The experimental results show that the maximum temperature rise of 4×4 chip array is less than 40 °C and the average temperature deviation is less than 10 °C at 500 W/cm². Different bifurcation angles and combinations can affect flow uniformity [21]. The flow uniformity is the best when the bifurcation angle is 180 ° [22]. The geometry of T joints and L bend can somewhat mutually compensate the pressure and temperature variations in the fluid, so that a smaller pressure loss and uniform temperature distribution can be achieved through the symmetrical construction design composed of the T joint and L bend [23].

Based on the fractal microchannel structure can reduce the pressure drop, improve the flow uniformity and the temperature uniformity of chip, this paper proposed to optimize the T-shaped and L-shaped corner structures of the fractal channel networks by introducing interior fillet structure (IFS). The four combined structures were compared and analyzed by computational fluid dynamic (CFD) modeling and simulation, and it was verified that the fractal channel with IFS can further reduce the pressure drop and improve the temperature uniformity of the chip array. The fractal microchannel heat sink test module with IFS was manufactured and assembled, and a test platform was built to test the hydro-thermal performance of the fractal microchannel heat sink under different conditions. The effectiveness of the simulation model was verified by the experimental and simulation data.

2. Numerical simulation

2.1. Numerical model

The fractal microchannel cold plate model proposed in this paper for heat dissipation of 4×4 chip array is shown in the Fig. 1(a). The 2×2 H-shaped fractal fluid distribution channels are used to supply coolant to 4×4 microchannel array units. The pressure drop in the microchannel heat sink is not limited to the frication pressure drop. The sudden contraction or expansion of the fluid will generate secondary flow and vortex when the fluid passes the T-shaped and L-shaped corner, which will increase the pressure drop and lead to coolant maldistribution. In this paper, the corner structure of the
microchannel cold plate is introduced the IFS to reduce the influence of secondary flow and vortex on pressure drop and flow uniformity caused by sudden change of flow direction. Figure 1(a) shows the radius of different interior fillets, and the central angle of different interior fillets are 90°. To realize the uniform liquid supply to the microchannel cold plate, a two-layer liquid supply structure was designed, respectively for the slot plate and coolant distribution plate. The slot plate realizes the four inlets and outlets liquid supply structure of the microchannel cold plate, and IFS is also to optimize the T-shaped and L-shaped corners of the coolant distribution plate. The schematic diagram of the three-dimensional multi-layer structure of the numerical model is shown is the Fig. 1(b), and the 4×4 chip array is bonded to the front of the microchannel cold plate through a thermal interface material with a thermal conductivity of 130 W/(m·K) and a thickness of 0.1 mm. The detailed data of each structure is shown in the Tab. 1.

![Figure 1. The schematic diagram of microchannel heat sink. (a) The microchannel cold plate. (b) The three-dimensional layered structure diagram](image)

![Table 1. The detailed dimensions of different structures](image)

<table>
<thead>
<tr>
<th>Material</th>
<th>Overall size (L × W × H mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>chip</td>
<td>Silicon</td>
</tr>
<tr>
<td>Microchannel cold plate</td>
<td>Silicon</td>
</tr>
<tr>
<td>Microchannel</td>
<td>-</td>
</tr>
<tr>
<td>Slot plate</td>
<td>Polymethyl methacrylate</td>
</tr>
<tr>
<td>Coolant distribution plate</td>
<td>Polymethyl methacrylate</td>
</tr>
</tbody>
</table>

To compare the pressure loss and flow velocity distribution of the structures with and without IFS, the four combined structures are shown in Tab. 2. The structure without IFS means that the IFS is not used at the T-shaped and L-shaped corners, and the without microchannel means that there are not microchannel array units in the silicon cold plate. The coolant flow paths of the four combined structures are shown in the Fig. 2.

![Figure 2. The flow path diagram of coolant in different combined structures](image)
Table 2. The structure types among the four combined structures

<table>
<thead>
<tr>
<th>Combined structure</th>
<th>Coolant distribution plate</th>
<th>Microchannel cold plate</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>without IFS</td>
<td>without microchannel and IFS</td>
</tr>
<tr>
<td>B</td>
<td>without IFS</td>
<td>with microchannel and without IFS</td>
</tr>
<tr>
<td>C</td>
<td>with IFS</td>
<td>without microchannel and with IFS</td>
</tr>
<tr>
<td>D</td>
<td>with IFS</td>
<td>with microchannel and IFS</td>
</tr>
</tbody>
</table>

2.2. Computational fluid dynamic simulation

The CFD modeling and simulation are performed by the finite element software (COMSOL\textsuperscript{TM}), and some assumptions are as follows:

(1) Steady-state, incompressible laminar flow.

(2) The effects of thermal radiation and fluid gravity are ignored.

(3) The thermophysical properties of the fluid vary with temperature but the thermophysical properties of solids are constant [11].

The corresponding governing equations are as follows.

Continuity equation:

$$\frac{\partial u}{\partial x} + \frac{\partial v}{\partial y} + \frac{\partial w}{\partial z} = 0$$  \hspace{1cm} (1)

Momentum equation:

$$\rho\left(u \frac{\partial u}{\partial x} + v \frac{\partial u}{\partial y} + w \frac{\partial u}{\partial z}\right) = -\frac{\partial P}{\partial x} + \mu \nabla^2 u$$ \hspace{1cm} (2)

$$\rho\left(u \frac{\partial v}{\partial x} + v \frac{\partial v}{\partial y} + w \frac{\partial v}{\partial z}\right) = -\frac{\partial P}{\partial y} + \mu \nabla^2 v$$ \hspace{1cm} (3)

$$\rho\left(u \frac{\partial w}{\partial x} + v \frac{\partial w}{\partial y} + w \frac{\partial w}{\partial z}\right) = -\frac{\partial P}{\partial z} + \mu \nabla^2 w$$ \hspace{1cm} (4)

Energy equation:

$$\rho C_p\left(u \frac{\partial T}{\partial x} + v \frac{\partial T}{\partial y} + w \frac{\partial T}{\partial z}\right) = k \nabla^2 T$$ \hspace{1cm} (5)

The flow rate ($f$) of the coolant was set to 80-480 ml/min and the inlet temperature was 20 °C. The heat flux ($q$) of the 4×4 chip array was set to 100-1000 W/cm\textsuperscript{2}. In addition, the pressure outlet was adopted at coolant outlet [24].

Set the grid cell size under physics-controlled mesh, and the grid independence was verified for combined structure D in different grid numbers (0.64, 0.95, 1.33, 2.12, 2.92, and 6.46 million). Grid independent results for pressure drop and the average temperature of 16 chips are shown in Fig. 3. When the grid number is 2.12 million, the exhibited maximum difference of the pressure drop and the average temperature of 16 chips is 0.76% and 0.66% compared with those of the finest grid case (6.46 million), respectively. Therefore, considering the accuracy of the results and the time cost of calculation, the 2.12 million grid cells were selected to execute the simulation analysis for combined structure D, and the corresponding grid cell size was in the coarse-mode. Similarly, the coarse-mode grid was used to simulate the combined structure A, B and C.
2.3. Simulation results and analysis

2.3.1 Pressure drop comparison of combined structures

The pressure drop and velocity distribution of combined A and C, B and D were studied in the flow rate range of 80-480 ml/min. As shown in Fig. 4, the velocity distribution of the combined structure D is more uniform than the combined structure B. This is because the T-shaped and L-shaped corners are optimized by the IFS to slow down the sudden change of fluid flow direction, thereby weakening the generation of secondary flow and vortex, and improving the flow uniformity of the coolant. Figure 4(c) shows the flow velocity distribution on the section line AA’ in Fig. 4(a) and (b), and the section line AA’ is the median line on the flow channel of corresponding section. As shown in Fig. 4(c), the sudden change of flow direction in combined structure B will cause stagnation pressure and increase the velocity when the coolant will enter the L-shaped corner, which will affect the coolant flow uniformity. The IFS slows down the sudden change of flow direction, so the flow velocity does not rise significantly and has high flow uniformity for combined structure D.

As shown in Fig. 5, more than 50% of the pressure drop comes from the fluid fractal channel by comparing A and B, C and D. This is because the fractal structure shortens the length of the microchannel, thus reducing the pressure drop of the microchannel. By comparing A and C, B and D, the fluid fractal structure with IFS can significantly reduce the pressure drop, and the pressure drop decreases more obviously with the increase of flow rate. The structure D reduces the pressure drop by 18.7% compared with B at 480 ml/min.
Figure 5. Comparison of pressure drop of four combined structures

2.3.2 Heat dissipation comparison of combined structures

Figure 6 shows the average temperature and standard deviation of temperature (σ) variations of 4×4 chip array in combined structure B and D at 480 ml/min and 100-1000 W/cm². The location and number distribution of 4×4 chip array is shown in Fig. 7(b). The standard deviation of temperature is a parameter index to evaluate the temperature uniformity of chip array. The smaller value of σ, the better temperature uniformity of chip array. The σ can be calculated by Eq. (6).

$$\sigma = \sqrt{\frac{1}{n} \sum_{i=1}^{n} (T_i - \bar{T})^2}$$  \hspace{1cm} (6)

Here, $T_i$ is the temperature of the chip numbered $i$ and $\bar{T}$ is the average temperature of all chips in chip array.

As shown in Fig. 6(a) and (b), the combined structure B and D have better temperature uniformity because the idealization of simulation boundary conditions, symmetry of structure and consistency of thermal interface materials. The maximum temperature difference of the 4×4 chip array is lower than 1.2 °C at 1000 W/cm² for both B and D, and the maximum temperature difference refers to the temperature difference between the chip with the highest and lowest temperature in the 4×4 chip array. Although the heat dissipation capability of the combined structure D is not significantly improved, the temperature uniformity is higher than the structure B. The temperature uniformity is improved more obviously with the increase of heat flux by comparing Fig. 6(a) and (b), which is due to the better flow uniformity of structure D. The standard deviation of temperature of structure D is 8.3% lower than the structure B at 1000 W/cm².
7

Figure 6. Combined structures B and D are compared for the heat dissipation performance of 4×4 chip array

3. Experiment

Based on the simulation results, the combined structure D with IFS has a better flow uniformity and temperature uniformity for the heat dissipation of 4×4 chip array. A test module was manufactured and assembled to verify the hydro-thermal performance of the combined structure D at different flow rates and heat fluxes.

3.1. Design, fabrication, and assembly of the test module

In this paper, the 4×4 chip array is the 1×1×0.4 mm TTC (thermal test chip). The TTC is test chip with array heating unit and temperature measuring unit made by CMOS (Complementary Metal Oxide Semiconductor) process. Each unit contains a temperature sensing diode (TSD) in the center and silicon resistor strips as the heat resource, which can characterize the thermal behavior of most power devices [25]. The microscope picture and circuit structure diagram of 1×1×0.4 mm TTC are shown in Fig. 7(c). The silicon microchannel cold plate was made by MEMS (Micro-Electro-Mechanical-System) process, the slot plate and coolant distribution plate were made by processing polymethyl methacrylate (PMMA) sheets.

The 4×4 TTC array was bonded to the front side of the microchannel cold plate by ATROX® 800HT2V (sliver conductive paste) with a thermal conductivity of 130 W/(m·K). A 0.5 mm thick PCB board with 4×4 holes to determine and match the corresponding bonding position. Laser-machined graphic polyimide film double-side adhesive (Kapton) 0.1 mm thick was used to bond and seal of microchannel cold plate and slot plate, slot plate and coolant distribution plate. The assembled test module is shown is Fig. 7(a).
Figure 7. (a) Test module assembly diagram. (b) The 4×4 TTC array of corresponding position distribution and number. (c) The microscope picture and circuit structure diagram of TTC

3.2. Flow loop

Fig. 8 shows the schematic diagram of the experimental flow loop. The deionized water was pumped to the test module by the infusion pump (Y-600, XYHY), and the TTCs were driven by direct current (DC) power (RIGOL DP832). Owing to the current limitation, the 4×4 TTC array was divided into four regions (region a, b, c, and d, and the location distribution of the four regions in Fig. 6(b)), which are respectively driven by four pairs of positive and negative ports of two direct current power supplies. In addition, each region contains a 2×2 TTC array. The inlet and outlet pressure drop and temperature difference of the test module were measured by the differential manometer (DPG409-050DWU, OMEGA) and T-type thermocouples respectively. The infrared imager (Flir T197415) was used to observe the temperature distribution of the 4×4 TTC array, and the standard temperature signal acquisition module (STSA-M) was used to collect the temperature sensing diode inside TTC.

Figure 8. The schematic diagram of the experimental flow loop

3.3. Data reduction

Although the heat transfer coefficient of natural cooling in air is very small (10⁻³ Wcm⁻²K) [26], it is necessary to estimate the heat loss \( Q_{\text{loss}} \) dissipated to the environment to determine the heat absorbed by the convection heat transfer of the coolant. The TTC temperature and corresponding thermal power were recorded in a steady-state condition when the thermal power was applied to TTC but without coolant in the test module. The best-fit line for heat loss is the following equation:

\[
Q_{\text{loss}} = 0.00979(T - 18.91)
\]
So, the power is transmitted to the coolant \( Q_{\text{trans}} \) can be calculated by the following equation.

\[
Q_{\text{trans}} = Q - Q_{\text{loss}} = IU - Q_{\text{loss}}
\]  

(8)

Where \( U \) and \( I \) are the input voltage and input current, respectively. In addition, the heat flux of 4 \( \times \) 4 TTC array is equal in this paper, and the corresponding calculation equation is shown in Eq. (9).

\[
q = \frac{Q}{A}
\]  

(9)

Here, \( A \) is the heating area of TTC (0.1 \( \times \) 0.1 cm\(^2\)), \( q \) is the heat flux of TTC.

### 3.4. Uncertainty

Table 3 summarizes the uncertainties of the experimental instruments used in this paper. To obtain the accurate TSD calibration temperature, the TTC was placed in the oven (ESPEC, SH-242) and the TSD positive and negative voltages were measured at 10 μA and different temperatures. In order to improve the accuracy of TTC temperature measurement, the temperature of the infrared imager was calibrated by STSA-M. The infrared temperature calibration curve is shown in Fig. 9. In this paper, the temperature measurement data are derived from the infrared temperature after STSA-M calibration. The accuracy of the TSD is calculated by the accuracy of the oven and the repeatability of the TSDs over time [27]. The other uncertain data comes from the sheets of manufactures.

According to the uncertainty analysis method by Moffat [28], the uncertainty of parameter heat flux \( q \) can be calculated by Eq. (10), and the uncertainty of the heat flux is about ±0.21%.

\[
\frac{\Delta q}{q} = \sqrt{\left(\frac{\Delta U}{U}\right)^2 + \left(\frac{\Delta I}{I}\right)^2}
\]  

(10)

| Table 3. Uncertainty and working range of experimental instruments |
|-------------------|------------------|---------|
| Parameter          | Instrument        | Range   | Uncertainty |
| Coolant temperature (°C) | Thermocouple    | -50–200 | ±1         |
| Pressure drop (kPa)      | Differential      | 0–350   | ±0.1%      |
| Volumetric flow rate (ml/min) | Infusion pump | 0–1000  | ±0.5%      |
| Power (W)                | Power supply     | 0–195   | 0.05% + 20 mV |
|                        |                  |         | 0.2% + 5 mA |
| TTC temperature (°C)     | TSD (calibrated) | -20-250 | ±0.5       |
3.5. Experimental results and analysis

3.5.1 The effect of heat flux

Figure 10(a) shows the experimental values of the average temperature of the 4×4 TTC array at 100-1000 W/cm² and 480 ml/min. The TTCs temperature increase linearly with the increase of heat flux. The maximum temperature difference of the 4×4 TTC array increases from 1.5 °C at 100 W/cm² to 11.68 °C at 1000 W/cm². In region a, b, c, d, the 2×2 TTC array in region b has the best temperature uniformity in Fig. 10(b), which may be due to the better flow uniformity in the H-shaped fractal channel networks and the better consistency of thermal interface material. As shown in Fig. 10(c), the standard deviation of temperature of 4×4 TTC array increases with the increase of heat flux, and it is below 3.5 °C at 1000 W/cm². The rising trend slows down possibly due to the fluctuation of the flow rate and DC power when the heat flux is 700-800 W/cm².

To verify the effectiveness of the simulation model, Figure 10(d) shows the comparison curves of simulation data and experimental data for the average temperature of 16 TTCs changing with heat flux. The error between the simulation data and the experimental data is within ±1.5%, which indicates the validity of the simulation model.
Figure 10. The effect of heat flux on temperature and temperature uniformity of 4×4 TTC array. (a) 4×4 TTC array average temperature distribution. (b) Standard deviation of temperature of the 4 regions. (c) Standard deviation of temperature of 4×4 TTC array. (d) Simulation and experimental values of all 4×4 TTC average temperatures.

3.5.2 The effect of flow rate

Figure 11(a) shows the variation of the average temperature of 4×4 TTC array with the heat flux at 1000 W/cm². As the flow rate increase, the TTCs average temperature gradually decrease, but the decreasing trend gradually becomes slower. The Reynolds number (Re) is low at the low flow rate, the heat of 4×4 TTC array cannot be absorbed by the coolant in time. With the increase of flow rate, the boundary layer thickness becomes thinner, and the heat transfer resistance between the coolant between coolant and microchannel wall decreases, thus enhancing the heat transfer inside the microchannel heat sink [29]. However, the decreasing trend of average temperature and standard deviation of temperature (Fig. 11(c)) becomes slower when the flow rate is higher than 400 ml/min, which may be because the coolant has already flowed out of the outlet of microchannel array unit before the heat transfer is completed. With the increase of flow rate, the maximum temperature difference of 4×4 TTC array gradually decreases from 12.43 °C at 160 ml/min to 10.94 °C at 480 ml/min. In Fig. 11(b), the region b has the smallest standard deviation of temperature and less fluctuation with flow rate. The temperature uniformity of region a, c and d is relatively poor, and the standard deviation of temperature improves significantly with the increase of flow rate. The data difference between Fig. 10 and Fig. 11 at 480 ml/min and 1000 W/cm² may be caused by bubbles and the fluctuation of the coolant flow rate and DC power. The temperature of some TTCs are higher than 100 °C at the low flow rate (160ml/min), which will cause some microchannel area to enter two-phase state, and the residual bubbles on the microchannel wall will affect the flow uniformity and heat dissipation. The fluctuation of flow velocity will affect the heat dissipation of heat sink, and the fluctuation of DC power will cause the difference of heat flux.
Figure 11. The effect of flow rate on temperature and temperature standard deviation of 4×4 TTC array

4. Conclusions

In this work, to achieve the high heat flux heat dissipation and improve the temperature uniformity of chip array, a H-shaped fractal microchannel networks by introducing the IFS into the T-shaped and L-shaped structures was proposed. The fractal microchannel heat sink of hydro-thermal performance was studied by simulation and experiment.

The simulation results show that more than 50% pressure drop is caused by the fractal channel because the T-shaped and L-shaped corners will cause stagnation pressure, so it is necessary to optimize the fractal channel structure to reduce the pressure drop. The IFS was proposed to alleviate the stagnation pressure and flow maldistribution caused by the sudden change of flow direction. The results show that the fractal microchannel heat sink with IFS can reduce the pressure drop by 18.7%, and the flow velocity distribution is more uniform. In addition, the temperature standard deviation of the fractal microchannel heat sink with IFS decreases by 8.3% at 480 ml/min and 1000 W/cm².

The 4×4 TTC array was employed to characterize the thermal behavior of the power chip array in experiment. The experimental results show that the fractal microchannel heat sink with IFS can realize that the average temperature and standard deviation of temperature of 4×4 TTC array is lower than 95 °C and 3.5 °C at 1000 W/cm², respectively. As the flow rate increases, the Re increases and the velocity boundary layer becomes thinner. The heat transfer resistance between the coolant and the microchannel wall will decrease, thus the temperature of the chip array decreases and the temperature uniformity will increase. However, the temperature uniformity improvement of the chip array is not obvious at the high flow rate (>400 ml/min). It is necessary to choose an appropriate flow rate to balance the pumping power and heat dissipation performance.

The H-shaped fractal microchannel networks with IFS not only can realize the high heat flux heat dissipation of chip array, but also can decrease the pressure drop and increase the temperature uniformity. Therefore, the research in this paper will contribute to the thermal management of the high heat flux heat dissipation and high temperature uniformity for chip array devices, such as T/R component array, LED (Light Emitting Diode) chip array, semiconductor laser, etc.

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Nomenclature

\( C_p \) constant pressure heat capacity, \( [\text{Jkg}^{-1}\text{C}^{-1}] \)

\( f \) flow rate, \( [\text{ml/min}] \)

\( H \) height, \( [\text{mm}] \)

\( L \) length, \( [\text{mm}] \)

\( P \) pressure, \( [\text{Pa}] \)

\( T \) temperature, \( [\text{°C}] \)

\( Q \) thermal power, \( [\text{W}] \)

\( q \) heat flux, \( [\text{Wcm}^{-2}] \)

\( u,v,w \) velocity components in x, y and z directions, \( [\text{ms}^{-1}] \)

\( W \) width, \( [\text{mm}] \)

\( r \) radius, \( [\text{mm}] \)

Greek symbols

\( \mu \) dynamic viscosity, \( [\text{kgm}^{-1}\text{s}^{-1}] \)

\( \rho \) density, \( [\text{kgm}^{-3}] \)

\( \sigma \) standard deviation of temperature, \( [\text{°C}] \)

Acronyms

IFS interior fillet structure

PMMA polymethyl methacrylate

TTC thermal test chip

References


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