COHERENT SYNTHESIS OF ULTRASHORT PULSE FIBER LASER BASED ON BALANCED DIFFERENCE METHOD

by

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The output power of the fiber laser can be increased by synthesizing the output beam, but the problem of low output power is caused by the poor ability of controlling bandwidth in the current synthesis research. Therefore, a coherent synthesis method of ultrashort pulse fiber laser based on balanced difference method is proposed. The balance difference of fiber combiner is divided into different modules, including data exchange and acquisition, circuit balancing, phase compensation, etc. Select appropriate ad conversion chip, use Ethernet chip W5300, design data exchange, ensure the normal use of data acquisition function, in the signal preprocessing module, use band-pass filter to filter out unnecessary frequency components, use AD603 to design front-end balancing circuit, design signal separation circuit, separate AC and DC signals, use active phase lock. The phase compensation of each laser is realized by the fixed technology, and the coherent synthesis of ultrashort pulse fiber laser is realized by the fiber combiner. The experimental results show that, compared with the traditional coherent synthesis method, the output power of the coherent combination method based on balanced difference method is about 900 kW, which has higher output power and better control bandwidth. It provides a theoretical basis for practical application.

Key words*: balanced difference method, pulse, fiber laser, coherent synthesis*

Introduction

Coherent synthesis technology of fiber laser or amplifier array is a research hotspot in the field of optoelectronic technology. It provides an effective way to obtain high power and high beam quality laser output, and will be an important research direction in the field of high-energy laser in the future [1]. Because of the small coupling area and the limited pump power, the output power of ordinary fiber laser is very low, which is usually in milliwatt level. With the development of cladding pumping technology, the output power of fiber laser has been greatly improved, which has reached kilowatt level [2]. With the further development of science and technology, it is expected to make a higher power fiber laser.

The key to the coherent synthesis of ultrashort pulse fiber laser is to correct the phase error between the coherent beams and realize the phase locking. The multi port output active phase-locked coherent synthesis based on the main oscillating power amplifier struc-

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ture is one of the best schemes of high-power beam synthesis. The heterodyne method interferes the N-path collimated beam with the reference light after frequency shift. The heterodyne information detected by N photodetectors is used to control n-phase modulators to compensate the phase error. In [3], the coherent combination method of pulsed fiber laser is studied. Based on the injection locked stimulated emission of diode, the comb frequency mode is allowed to sprout with enough power amplification, but the original comb frequency stability is not lost. In [4], a multichannel optical frequency synthesizer is proposed, which can directly generate a very stable CW laser from the optical comb of an erbium-doped fiber oscillator. It can provide stable optical frequency. The principle is relatively simple, but the module is relatively complex and the optical path adjustment is difficult.

At present, the ability of the coherent synthesis method of ultrashort pulse fiber laser to control the bandwidth is poor, resulting in the low output power of the far-field spot. Therefore, the balanced difference method is used to process the optical signal, improve the anti-interference of the signal, and make the coherent synthesis method of ultrashort pulse fiber laser have the ability of normal bandwidth control.

Coherent synthesis of ultrashort pulse fiber laser

Photoelectric signal acquisition function design

The preprocessing based on balanced difference method includes signal preprocessing module and data acquisition module, as shown in fig. 1.

The whole signal processing part can be divided into two parts: signal preprocessing and data acquisition. The signal preprocessing is mainly realized by analog signal processing mode [5], including low-pass filter, measurement amplifier, programmable amplifier, add and subtract arithmetic, and band-pass filter. The digital signal processing mode selected by data acquisition circuit is mainly composed of data acquisition chip, signal input/output buffer, reset circuit, serial communication interface, *etc*.

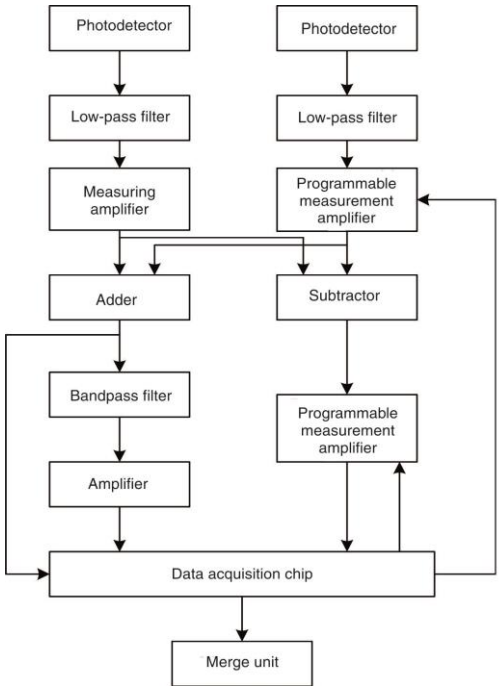

Figure 1. Signal acquisition and processing flow

Design of data acquisition chip

The AD conversion module is the core of data acquisition chip, which has a great impact on the overall performance. At present, there are many kinds of AD conversion methods with different performances, mainly including the following types: double oblique integration, successive approximation, and lightning type AD conversion. Among them, the lightning AD conversion mode has the fastest speed and the most expensive price, but the lightning AD conversion mode usually has low accuracy and resolution, so it is not suitable to be used in the high accuracy sampling module [6]. The double oblique integral type has high accuracy and low price, but its speed is slow and it is diffi-

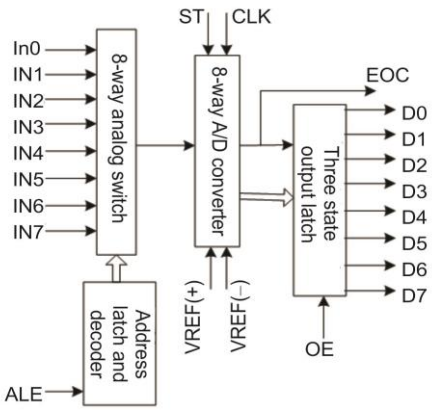

Figure 2. Schematic diagram of data acquisition chip;
D0-D7 – 8-bit digital output pin, IN0-IN7 – 8-bit analog output pin, VREF(+) – reference voltage positive terminal, VPEF(–) – reference voltage negative terminal, ST – A/D conversion start signal input terminal, ALE – address latch enable signal input, EOC – conversion end signal output pin is low at the beginning of conversion and high at the end of conversion, OE – output permission control terminal is used to open the three state data output latch, and CLK – external clock source

cult to meet the requirements. The successive approximation type has the advantages of fast speed, moderate price, high resolution and accuracy, so the successive approximation type data acquisition chip should be selected here [7], The schematic diagram of data acquisition chip is shown in fig. 2.

The selection and analysis of ad bits are as follows: for *n* bit AD, if the quantization unit is *e* and the maximum ad range is *R*, then the maximum quantization error will be:

$$\varepsilon = \pm\frac{e}{2} = \pm\frac{R}{2^n * 2} = \frac{R}{2^{n+1}} \tag{1}$$

Since the quantization of analog signals generally introduces additional noise, when the quantization noise is random noise, the quantization error *i* of each sample point obeys the uniform distribution, and *f*(*t*) is set as its probability density function, so the quantization noise power can be expressed as:

$$\rho = \int_{-e/2}^{e/2} i^2 s(t)\,dt \tag{2}$$

where ρ represents the effective value or measurement inaccuracy of the quantization noise within the measurement bandwidth.

It can be seen from the previous formula that the total noise after digitization does not need complex calculation in the chip after considering the acquisition. Therefore, in the design of data acquisition function, adc812 is used as the core chip of data acquisition. The adc812 controls ADC, DAC and other peripheral chips through internal special function registers, so its ad conversion program and DA conversion program are simpler and easier than the traditional structure of 8051 plus peripheral chips. The internal 12 bit AD conversion cycle is only 4S, which is several times faster than the common AD574 (conversion cycle 22s) [8]. After rough estimation, if a conventional chip is used to form a data acquisition module with the same performance as adc812, one chip of 8031, one chip of ad57427642816, two chips of dac80, and several chips of decoder, register and multi-channel switch are needed [9]. Not only the price of these chips is much higher than that of adc812, but also the cost of a single PCB is roughly the same as that of adc812. Its kernel is inte18051, which is familiar to technicians. The existing software can be directly transplanted and its programming is relatively simple. It can be programmed by general programmer or by loading program directly through serial port of PC. Ad company provides adc812 with complete C language and assembly language to develop simulation software and hardware debugging module tools. Simulation debugging software has a popular WINDOWS user interface and is very flexible and convenient to use. In short, it is a high performance data acquisition chip with excellent performance, low price and complete development means. Because of the previous functions, adc812 is used as the core chip of this module.

The AD conversion block in adc812 integrates a fast, 8-Channel, 12 bit, single power ADC. It is a capacitor 12 bit power supply ADC with successive approximation conversion technology. The conversion time is 5S and the acquisition rate can be as high as 200 kHz. This module provides users with multichannel multiplexer, sample holder, on-chip reference power supply, calibration circuit, AD converter and other components, and all these components can be easily set through three special function registers [10]. There is a factory programmed calibration coefficient in the chip, which is automatically downloaded to the ADC when power is on to ensure the best ad conversion performance. If internal reference is used, 100 nF capacitance shall be connected between VREF and CREF pin and analog ground and for decoupling. These decoupling capacitors should be placed close to VREF and CREF pins. It should be noted that the internal reference source is in power down state before the ADC or DAC enters into operation. When the reference voltage is provided by an off chip reference source, simply connect the external reference voltage to the VREF pin. In order to ensure the technical index of adc812, the external reference voltage is set in the range of 2.3 V ~ avdd pin voltage. This not only avoids the lack of accuracy of AD conversion result caused by reference voltage fluctuation, but also omits one-step division operation by the ratio of two channels of data. Analog voltage input range of ADC is 0 ~ VREF. In this range, the designed code jump occurs in the middle of a continuous integer LSB value. When VREF = 2.5 V, the output code is a direct binary number. The ideal input/output conversion characteristics in the range of 0 ~ VREF are shown in fig. 3.

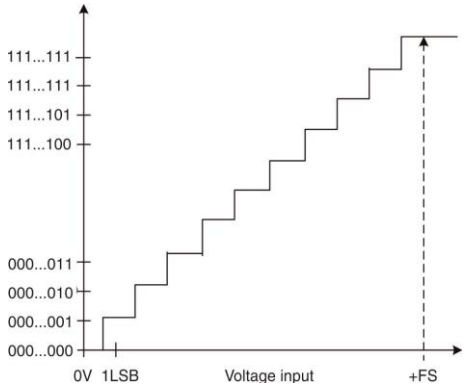

Figure 3. Input/output conversion characteristics of adc812

Although the AC component in the input signal is very small, the order of magnitude is 10-3, but the AC/DC separation has been successfully carried out, and the AC component amplitude can be amplified to the measuring range for gold plating. Only selecting the appropriate a/D converter can make good use of the ad bits and provide the absolute accuracy of the whole data acquisition module.

Data exchange module design

The data exchange module exchanges data with the upper computer through the network port. It has two functions: one is to transmit the data sent from adc812 to the upper computer for display, processing and analysis. The other is to receive the commands and parameters sent from the upper computer and give them to adc812 for control and calculation. Because the image transmission is not involved in the coherent synthesis of ultrashort pulse fiber laser, and the amount of data is small, the module uses a 10/100M Ethernet chip W5300, which integrates TCP/IP Ethernet controller, MAC and TCP/IP protocol stack inside the chip, so it can send and receive data conveniently. In addition, considering that the research target is point-to-point communication, the mode is single and the environment is good, UDP protocol is adopted for communication.

After W5300 initialization, it can respond to Ping request, and then complete the initialization of socket to be used for communication. Set the socket port number, destination hardware address, destination port number, destination IP address, interrupt mask register and mode register, and W5300 can carry out data transmission of Ethernet.

Because W5300 processes all communication protocols internally, the receiving data flow and sending data flow can be basically simplified as a fixed combination of read register operation and write register operation, and the format of receiving data packet is also very simple. The signals of W5300 chip and adc812 chip interface include seven groups: Address bus (addr9-0), data bus (data (15:0), chip select signal $\overline{CS}$, read enable signal $\overline{RD}$, write enable signal $\overline{WR}$, interrupt request output INT, and reset signal $\overline{RESET}$.

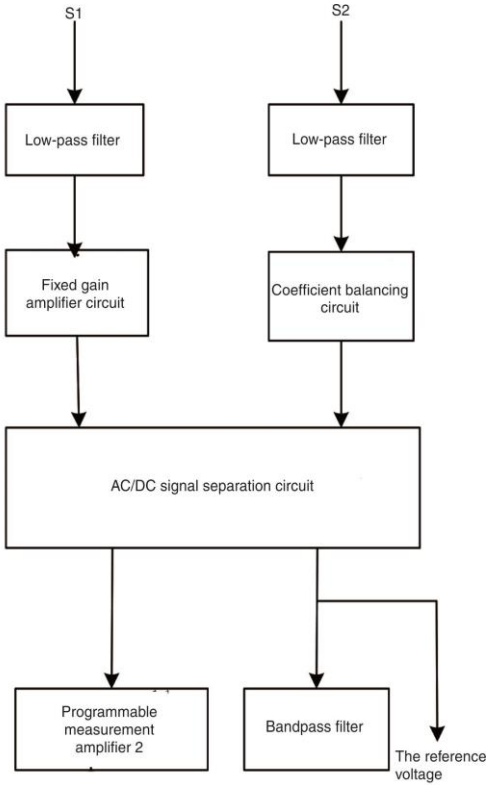

Figure 4. Structure of signal preprocessing part

Signal preprocessing

Signal preprocessing circuit mainly includes four parts: filter design, front-end coefficient balancing circuit design, AC/DC signal separation circuit design and fixed gain amplifier circuit design, as shown in fig. 4.

Because the input signal may have clutter on the power grid, and the sampling theorem requires that the bandwidth of the sampled signal must be limited to avoid frequency aliasing, so it is necessary to use the filter circuit to filter out the unwanted frequency components to meet this requirement [11]. At present, active mode is generally used in filter design, which is characterized by strong load capacity, good filter characteristics and certain amplification effect. In the design of signal preprocessing, active filter is used in both filters, which is composed of max275.

Because the AD sampling frequency is 4 K, according to the sampling theorem, the cutoff frequency f_0 = 1 kHz is set, and the gain amplification factor is 1. In this way, using max275 to design the filter can be reduced to the calculation of resistance. The resistance calculation formula of four external resistances is:

$$R_1 = \frac{2\times10^9}{h_0\zeta}\frac{R_x}{R_y} \tag{3}$$

$$R_2 = \frac{2\times10^9}{h_0} \tag{4}$$

$$R_3 = \frac{2\times10^9 K}{h_0\zeta}\frac{R_x}{R_y} \tag{5}$$

$$R_4 = R_2 - 5K \tag{6}$$

where h_0 is the cut-off frequency, ζ – the gain of the low-pass filter, and K – the quality factor. The value of R_x/R_y depends on the connection method of frequency control terminal FC. If FC

is grounded R_x/R_y = 1/5, if FC is connected with positive power supply R_x/R_y = 4, if FC is connected with negative power supply R_x/R_y = 1/25. If the external resistance R_1~R_4 is too large or too small, the latter two methods can be used to adjust the resistance. For the design of low-pass Butterworth filter, K = 0.707 can be substituted into the above formula to calculate its resistance, so the design is very convenient.

The band-pass filter is designed to isolate the direct flow and detect the AC, which is convenient to control the program-controlled gain after AD acquisition. As there has been a low-pass filter before, it can be satisfied that the second-order voltage controlled active high pass filter and low-pass filter are designed by two OP amplifiers of op2177 and combined into band-pass filter. The circuit diagram of band-pass filter is shown in fig. 5.

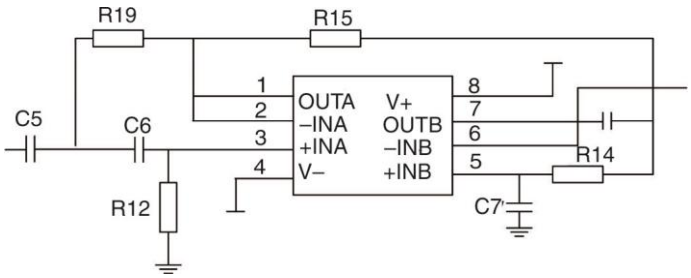

Figure 5. Circuit diagram of band-pass filter

Among them, U_{10A}, C_5, C_6, R_6, and R_2 constitute a high pass filter, and its cut-off frequency is:

$$h_1 = \frac{1}{2\pi\sqrt{C_5 C_6 R_6 R_2}} \tag{7}$$

If U_{10B}, C_7, C_8, R_4, and R_5 AA form a low-pass filter, the cut-off frequency is:

$$h_2 = \frac{1}{2\pi\sqrt{C_7 C_8 R_4 R_5}} \tag{8}$$

In this way, the passband of band-pass filter can eliminate DC and keep 50 Hz AC, which ensures the accuracy of the data acquisition chip to the program-controlled gain amplifier.

In the design of signal preprocessing, the gain of the amplifier must be adjusted according to the change of the input signal, so that the front-end coefficients of the signal are equal, and the self balancing function can be realized, so as to eliminate the influence of the loss coefficient. This requires the use of programmable amplifiers, data acquisition chip by controlling it and then adjust the signal coefficient, get the required signal [12]. When 5-pin and 7-pin are short circuited, the output gain of AD603 can be expressed as 40 V_G + 10, and the gain range is – 10 ~ + 30 dB. When pin-5 and pin-7 are disconnected, the output gain can be expressed as 40 V_G + 30, and the gain range is 10~50 dB. If the resistance is connected at 5-pin and 7-pin, the output gain range will be between them. The gain of the whole AD603 can be calculated by:

$$Gain(dB) = 40V_G + G \tag{9}$$

where V_G represents the voltage difference between pins 1 and 2, and G represents the starting point of gain. Under different feedback networks, G is different. The previous three connec-

tion methods *G* are l0 dB, 30 dB, and 20 dB, respectively. It should be noted that the effective range of control voltage of AD603 is only – 0.5 V to + 0.5 V. When the voltage difference between pins 1 and 2 is greater than + 0.5 V, it is equivalent to + 0.5 V. When the voltage difference is less than – 0.5 V, it is equivalent to – 0.5 V. As the output pin is 7-pin, the positive and negative power supply is 8-pin and 6-pin, so be careful when measuring the output. Once the output terminal is short circuited with the power supply terminal, the chip will be permanently damaged.

Experimental study

Aiming at the problem of low output power in the traditional coherent synthesis method of ultrashort pulse fiber laser, the output power is taken as the evaluation index in the experimental study of coherent synthesis method. The output power is a quantity describing the energy concentration degree of far-field facula, whose value is between 0 and 1. The larger the value is, the better the energy concentration degree of far-field facula is. The output power is defined:

$$PIB = \frac{\iint_{\pi r} p(x,y)}{\iint_{\infty} p(x,y)} \tag{10}$$

where $p(x,y)$ represents the light intensity distribution of far-field spot and r represents the radius of circular barrel. In the experiment, the signal detected by PD is the output power within the pinhole range. The pinhole size represents the barrel size of the calculated output power. The pinhole size used for the phase-locked control is 20 m.

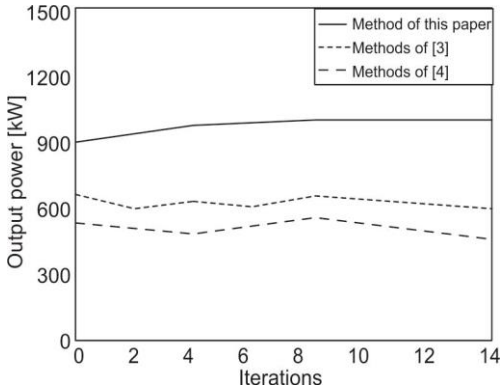

Figure 6. Compare the experimental results

In order to verify the effectiveness of the coherent combination method of ultrashort pulse fiber laser based on balanced difference method in this paper, the method proposed in [3, 4] is taken as the contrast object, and the contrast experiment is carried out. The experimental results are shown in fig. 6.

It can be seen from fig. 6 that the output power of the two literature methods is maintained at about 600 kW. Compared with the two literature methods, the output power of the method in this paper is maintained at about 900 kW, the output power is larger, and the energy concentration of far-field spot is better.

Conclusion

This paper designs the coherent synthesis method of ultrashort pulse fiber laser based on the balanced difference method. By using the balanced difference method to process the photoelectric signal, the accuracy of the signal can be guaranteed, and the problems existing in the traditional coherent synthesis method of ultrashort pulse fiber laser can be solved, which will provide some help for the follow-up research of ultrashort pulse fiber laser and promote the development of laser technology.But in this study, the experimental test index is less, not applied in practical operation, in the future development, further improve here.

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