THERMAL MANAGEMENT OF 3-D INTEGRATED CIRCUITS WITH SPECIAL STRUCTURES

by

***Kang-Jia WANG*[a] *and Cui-Ling LI*[b,*]**

[a] School of Physics and Electronic Information Engineering, Henan Polytechnic University, Jiaozuo, China
[b] Information Engineering School, Huizhou Economics and Polytechnic College, Huizhou, China

Original scientific paper
https://doi.org/10.2298/TSCI200115109W

Different stacked structures affect greatly the temperature distribution of a 3-D integrated circuit, and an optimal structure is much needed to reduce the maximal temperature. This paper suggests a numerical approach to such structures with different heat source distributions. The results show that an optimal stacked structure can reduce the maximum temperature by 8.7 ℃.

Key words: *thermal, 3-D integrated circuit, thermal management, special structures*

Introduction

By using the through silicon vias (TSV) to realize vertical electrical interconnection of different layers, the 3-D integrated circuits (3-D IC) provide a promising option to build high performance compact IC, which have attracted a lot of attention in the academic community and the electronic industry [1-4]. Compared with the traditional 2-D IC, the 3-D IC have many advantages in low power consumption, good noise immunity, large packaging density and fast speed due to reduced wire length/low wire capacitance [5-7]. However, the 3-D stacking structure greatly increases the power density in a unit volume, which easily leads to high working temperature, as a result, it will affects the normal operation of the chip, and even leads to the thermal failure. Therefore, the thermal management of the 3-D IC faces great challenges, and effective cooling methods have become one of the key issues in the development of 3-D IC [8-15].

There have been a lot of research results achieved on the thermal management of 3-D IC with regular structure. In [16], an equivalent anisotropic thermal model was proposed and used to reduce the computational time for the complicated numerical integration, resulting in overcoming the complex nature of the TSV structure. In [17], a new stochastic based genetic algorithm was proposed for reducing the thermal estimations. A machine learning (ML)-based control method was proposed and applied to 3-D IC with the tier-specific microfluidic heat sink in [18]. In [19], the Manchester Thermal Analyzer (MTA) was used to give fast and highly accurate thermal simulation for the complex physical structure. Alqahtani, *et al.* [20] proposed a simulation flow to accurately simulate TSV effects on 3-D IC, and found that the peak temperature of 3-D Nehalem could be reduced by 5-25%. Zajac, *et al.* [21] pro-

* Corresponding author, e-mail: licl2003@outlook.com

posed a novel model for thermal simulation of IC cooled with integrated micro-channels which significantly reduced the simulation time, and a very good accuracy was obtained with a maximum error of 3.3 °C. Pi, *et al.* [22] proposed a fast and implementable full chip-scale numerical simulation method for thermal management of 3-D-IC by using the compact thermal resistance network and found that the proposed method could improve the simulation accuracy (temperature difference < 7.5%) and considerable computational cost reduction (grid number reduced by > 77%). Lu, *et al.* [23] presented a temperature gradient-aware thermal simulator for 3-D IC (called 3-D-TarGA) at the architectural level. Xiao, *et al.* [24] proposed a fast and accurate equivalent approach based on finite element analysis (FEA) for estimating the equivalent thermal conductivity of 3-D IC device, and the approach was validated by 3-D FEA method. In [25], an analytical thermal model for 3-D IC with micro-channel cooling was considered, and the proposed model produced a maximal relative error less than 4.0%. Wang and Sun [26] suggested a micro-channel cooling model for 3-D IC considering TSV, and revealed that TSV could effectively improve the heat dissipation, and its maximal temperature reduction was about 10.75%. In [27], the H^2-based mathematical framework was applied to FE-based transient analysis of thermal parabolic partial differential equations, showing that the method was much more memory efficient and speedup than these in literature.

In fact, not all the 3-D IC are regular structures, and some may have special structures, such as pyramid structure. This paper focuses on studying the effect of different stacking structures on temperature distribution of 3-D IC with special structures. The obtained results are expected to be helpful for the 3-D IC' optimal design.

The physical thermal model

Figure 1 shows the general physical and thermal model of the 3-D IC, where the different layers are bonded by the bonding layer to form the 3-D structure, and different layers are inter-connected by the TSV to achieve the electrical interconnection. The number of devices that can be integrated within the system is limited as the following formula [28]:

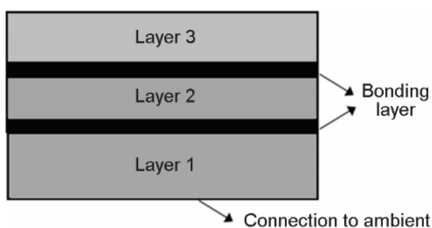


Figure 1. The 3-D IC model

$$\frac{\alpha N_G E}{t_{pd}} \le g\Delta T \tag{1}$$

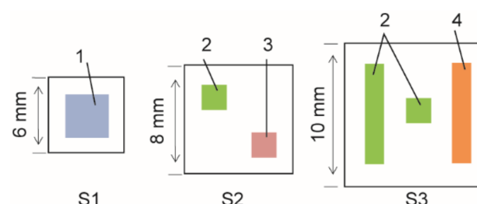
where N_G is the number of gates that can be integrated within a system with a clock period t_{pd}, α – the activity rate, E – the energy dissipation, g – the average thermal conductance, and ΔT – the temperature gradient between the dissipating elements and the ambient air.

Model establishment

Figure 2 shows the three different layers with different heat source distribution and sizes. The different thermal parameters of three layers S1, S2, and S3 are set as: the density, thermal conductivity and specific heat capacity of S1 are 1200 kg/m^3, 80 W/m°C, 200 J/kg°C, S2 are 1500 kg/m^3, 100 W/m°C, 150 J/kg°C, S3 are 1000 kg/m^3, 50 W/m°C, 300 J/kg°C, respectively.

According to the heat source distribution of each layer in fig. 2, we use different stacking structures to establish the corresponding numerical models as shown in fig. 3, where

Figure 2. Different layers and their heat sources; *1 – 2·10⁸ W/m³, 2 – 5·10⁸ W/m³, 3 – 1·10⁹ W/m³, 4 – 1.25·10⁸ W/m³*



the different layers have the same height of 2 mm. The model of fig. 3(a) results in about 16701 nodes and 2628 elements by meshing which is plotted in fig. 4(a). Figure 4(b) illustrates the meshed results of the model of fig. 3(b), there are about 16841 nodes and 2652 elements.

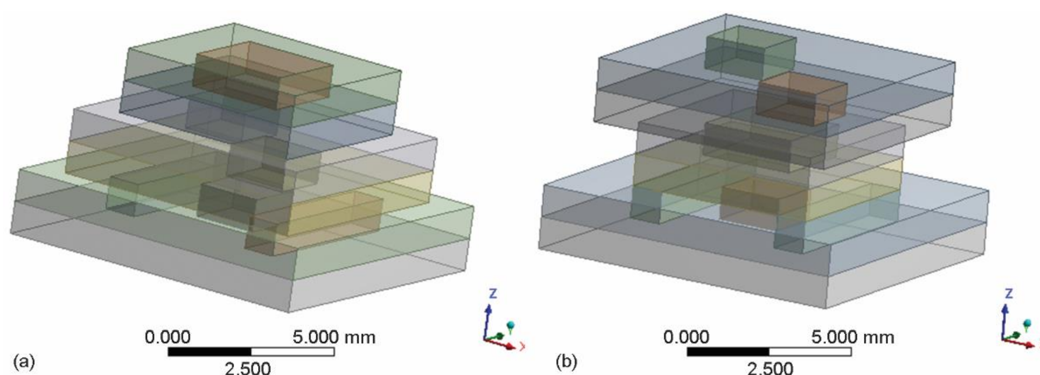


Figure 3. The 3-D IC of different stacked forms

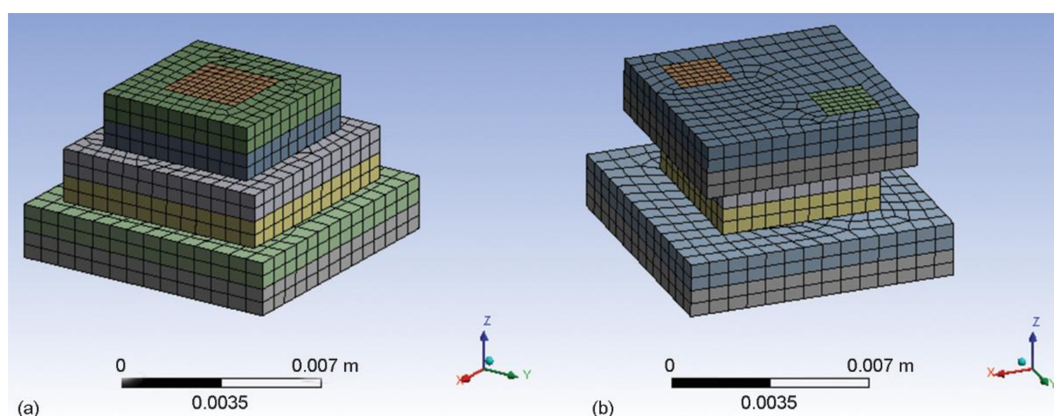


Figure 4. The meshed models

After meshing the models, we simulate the models by setting initial temperature as 22 °C, convection coefficient of the top and bottom surfaces as 1200 W/m^2°C and 2000 W/m^2°C, respectively. All the other side surfaces are assigned to be adiabatic. The simulated results are shown in fig. 5. It can be found that the maximum and minimum temperatures of Model 1 and Model 2 are 86.356 °C, 73.621 °C, and 82.727 °C, 64.905 °C, respectively. By comparing figs. 5(a) and 5(b), it can be easily seen that the temperature have

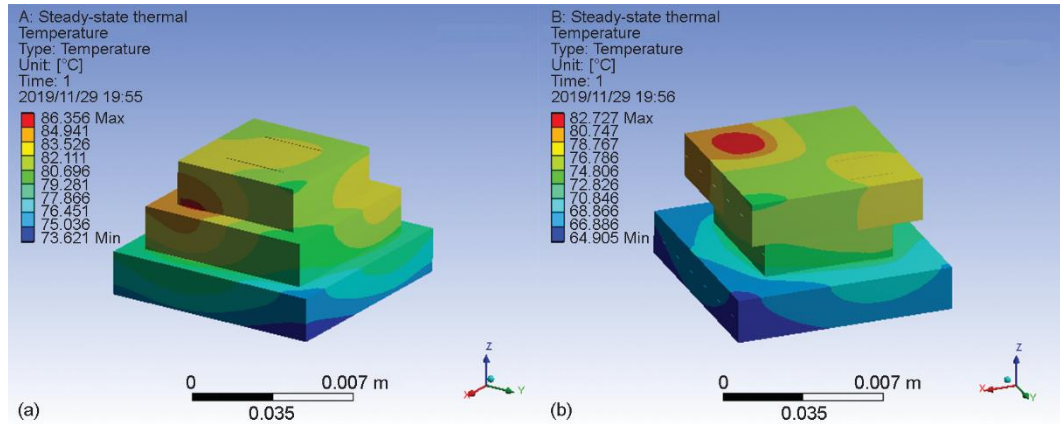


Figure 5. The simulated results

a decline after rearranging the stacking form of different layers, where the decline of the maximum temperature is 3.629 °C and the minimum temperature is 8.716 °C, revealing that the different stacked structures have an effect on the temperature distribution of the 3-D IC.

Conclusion

In this paper, the thermal optimization of 3-D IC is studied by rearranging the stacking form. The obtained results show that the maximum and minimum temperature can be declined by rearranging the stacking form, where the maximum temperature can be reduced by 8.7 °C. The results presented in this paper are expected to aid in the development of thermal design guidelines for the 3-D IC.

Acknowledgment

This work is supported by Program of Henan Polytechnic University (No. B2018-40), the Fundamental Research Funds for the Universities of Henan Province (NSFRF210324), Innovative Scientists and Technicians Team of Henan Provincial High Education (21IRTSTHN016) and Key Project of Scientific and Technology Research of Henan Province (212102210224).

References

[1] Zhao, Y., *et al.*, Thermal and Wirelength Optimization With TSV Assignment for 3-D-IC, *IEEE Transactions On Electron Devices, 66* (2019), 1, pp. 625-632
[2] Wang, K. J., *et al.*, Thermal Management of the Through Silicon Vias In 3-D Integrated Circuits, *Thermal Science, 23* (2019), 4, pp. 2157-2162
[3] Hou, L. G., A Method to Alleviate Hot Spot Problem in 3-D IC, *Microelectronic Engineering, 190* (2018), Apr., pp. 19-27
[4] Wang, K. J., *et al.*, Integrated Microchannel Cooling In A Three Dimensional Integrated Circuit A Thermal Management, *Thermal Science*, *20* (2017), 3, pp. 899-902
[5] Wang, K. J., *et al.*, Thermal Management Of The Hotspots In 3-D Integrated Circuits, *Thermal Science, 22* (2018), 4, pp. 1685-1690
[6] Lu, T., *et al.*, TSV-Based 3-D IC: Design Methods and Tools, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *36* (2017), 10, pp. 1593-1619
[7] Wang, K. J., Wang, G. D., Variational Principle and Approximate Solution for the Fractal Generalized Benjamin-Bona-Mahony-Burgers Equation in Fluid Mechanics, *Fractals,* On-line first, https://doi.org/10.1142/S0218348X21500754, 2021

[8] Feng, Z., Li, P., Fast Thermal Analysis on GPU for 3-D IC With Integrated Microchannel Cooling, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *21* (2013), 8, pp. 1526-1539
[9] Wang, K. J., A New Fractional Nonlinear Singular Heat Conduction Model for the Human Head Considering the Effect of Febrifuge, *Eur. Phys. J. Plus, 135* (2020), Nov., ID 871
[10] Patti, R. S., 3-D Integrated Circuits and the Future of System-On-Chip Designs, *Proceedings of the IEEE, 94* (2006), 6, pp. 1214-1224
[11] YOON, J. K., *et al.*, Thermal Characterization Of Interlayer Microfluidic Cooling Of 3-D Integrated Circuits With Nonuniform Heat Flux, *Journal of Heat Transfer, 132* (2010), 4, pp. 041009-041018
[12] Banerjee, K.. Mehrotra, A., Global (Interconnect) Warming, *IEEE Circuits Devices Mag., 17* (2001), 5, pp. 16-32
[13] Wang, K. J., *et al.*, An Analytical Model for Steady-state and Transient Temperature Fields in 3-D Integrated Circuits, *IEEE Transactions on Components Packaging & Manufacturing Technology, 6* (2016), 7, pp. 1028-1041
[14] Wang, K. J., Variational Principle and Approximate Solution for the Generalized Burgers-Huxley Equation with Fractal Derivative, *Fractals*, On-line first, https://doi.org/10.1142/S0218348X21500444, 2021
[15] Bagnall, K. R., *et al.*, Analytical Solution for Temperature Rise in Complex Multilayer Structures with Discrete Heat Sources, *IEEE Transactions on Components Packaging & Manufacturing Technology., 4* (2014), 5, pp. 817-830
[16] Chai, J., *et al.,* An Effective Approach for Thermal Performance Analysis of 3-D Integrated Circuits With Through-Silicon Vias, *IEEE Transactions on Components, Packaging and Manufacturing Technology, 9* (2019), 5, pp. 877-887
[17] Sivakumar, P., *et al.,* Optimization of Thermal Aware Multilevel Routing for 3-D IC, *Analog Integrated Circuits and Signal Processing, 103* (2020), Oct., pp. 131-142
[18] Li, Y. S., *et al.,* Dynamic Thermal Management for 3-D IC With Time-Dependent Power Map Using Microchannel Cooling and Machine Learning, *IEEE Transactions on Components, Packaging and Manufacturing Technology, 9* (2019), 7, pp. 1244-1252
[19] Ladenheim, S., *et al.,* The MTA: An Advanced and Versatile Thermal Simulator for Integrated Systems, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *37* (2018), 12, pp. 3123-3136
[20] Alqahtani, A., *et al.,* System-Level Analysis of 3-D IC with Thermal TSV, *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, *14* (2018), 3, pp. 1-16
[21] Zając, P., Napieralski, A., Novel Thermal Model of Microchannel Cooling System Designed for Fast Simulation of Liquid-Cooled IC, *MicroelectronIC Reliability, 87,* (2018), Aug., pp. 245-258
[22] Pi, Y., *et al.,* Anisotropic Equivalent Thermal Conductivity Model for Efficient and Accurate Full-Chip-Scale Numerical Simulation of 3-D Stacked IC, *International Journal of Heat and Mass Transfer*, *120* (2018), May, pp. 361-378
[23] Lu, L. Y., Chiou, L. Y., Temperature gradient-Aware Thermal Simulator for 3-D Integrated Circuits, *IET Computers & Digital Techniques, 11 (2017)*, 5, pp. 190-196
[24] Xiao, C., *et al.,* An Effective and Efficient Numerical Method for Thermal Management in 3-D Stacked Integrated Circuits, *Applied Thermal Engineering, 121* (2017), July, pp. 200-209
[25] Wang, K. J., *et al.,* An Analytical Thermal Model for 3-D Integrated Circuits with Integrated Micro-Channel Cooling, *Thermal Science, 21* (2017), 4, pp. 1601-1606
[26] Wang, K. J., Sun, H. C., A Micro-Channel Cooling Model For a 3-D Integrated Circuit Considering Through-silicon Vias, *Micro And Nanosystems*, *13* (2021), 1, pp. 49-54
[27] Chen, H. B., *et al.* H^2-Matrix-Based Finite Element Linear Solver for Fast Transient Thermal Analysis of High-Performance IC, *International Journal of Circuit Theory and Applications, 43* (2015), 12, pp. 1953-1970
[28] Nagata, M., Limitations, Innovaions, and Challenges of Circuits and Devices into a Half Micrometer and Beyond, *IEEE Journal of Solid-State Circuits, 27* (1992), 4, pp. 465-472

Paper submitted: January 15, 2020
Paper revised: June 20, 2020
Paper accepted: June 20, 2020
© 2021 Society of Thermal Engineers of Serbia.
Published by the Vinča Institute of Nuclear Sciences, Belgrade, Serbia.
This is an open access article distributed under the CC BY-NC-ND 4.0 terms and conditions.