THERMAL OPTIMIZATION OF A 3-D INTEGRATED CIRCUIT

by

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In a 3-D integrated circuit the heat source distribution has a huge effect on the temperature distribution, so an optimal heat source distribution is needed. This paper gives a numerical approach to its thermal optimization, the result can be used for 3-D integrated circuit optimal design.

Key words: *thermal, 3-D integrated circuit, thermal optimization*

Introduction

In the latest decade, the 3-D integrated circuit (3-D IC) technology has attracted wide attention in the semiconductor industry [1-6], which has been emerging as a powerful tool for satisfying the requirement of integrated circuit packaging so as to extend greatly the space of IC development and overcome completely the drawbacks of 2-D IC. The way to realization of the 3-D packaging structure is stacking, which has many advantages in an increased speed, a large packaging density, a low weight/volume, and reduced power consumption and footprint [7-16]. While the package density increases, the heat quantity in each unit volume becomes higher, which will greatly increase the working temperature of the device. Excessive working temperature will seriously affect the stability and reliability of the device, and even lead to the thermal failure. The problems of heat dissipation in 3-D IC are more serious and catching lots of attentions than those in the traditional single IC package. Hence, thermal management for 3-D IC is becoming a major concern [17-21].

Thermal management of 3-D IC has been widely recognized as a significant technology for widespread implementation of the 3-D IC technology. In recent years, a lot of achievements have been developed for the thermal management of 3-D IC. In [22], the domain decomposition method was used to compute the temperature fields. In [23], the Green's function was used to compute the thermal distribution of the 3-D IC, where the method was not only applicable to transient thermal problems, but also to the steady-state thermal problems. The thermal through silicon vias (TTSV) combined with micro-channel cooling method was used to solve the hotspot problems in [24]. In this paper, we mainly study the thermal optimization problems in 3-D IC by rearranging the heat source distributions. The results show that the maximum temperature can be reduced by about 4.99%. The results presented in this paper are expected to aid in the development of thermal design guidelines for 3-D IC.

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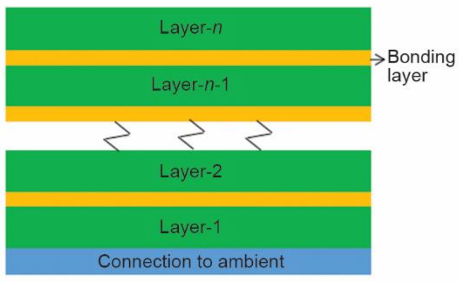

Figure 1. The 3-D IC model

Analysis model

Figure 1 shows the general physical and thermal model of the 3-D IC, where the different layers are bonded by the bonding layer to form a 3-D structure, and different layers are inter-connected by the TSV to achieve the electrical interconnection. The number of devices that can be integrated within the system is limited as the following formula [25]:

$$\frac{\alpha N_{\mathrm{G}} E}{t_{pd}} \le g\Delta T \tag{1}$$

where N_{G} is the number of gates that can be integrated within a system with a clock period, t_{pd}, α – the activity rate, E – the energy dissipation, g – the average thermal conductance, and ΔT – the temperature gradient between the dissipating elements and the ambient air.

Heat flow in a control volume of a solid in the 3-D IC with an isotropic thermal conductivity can be governed by the following equation [26]:

$$C_{\mathrm{v}}\frac{\mathrm{d}T}{\mathrm{d}t} + (-k\nabla^2 T) = \dot{q} \tag{2}$$

where C_{v} is the volumetric specific heat of the material, T – the temperature of the control volume, k – the thermal conductivity of the material, $\dot{q}$ – the volumetric rate of heat generation inside the volume. This equation can be solved by various analytical methods [14, 15], and the Taylor series method is the simplest one [27].

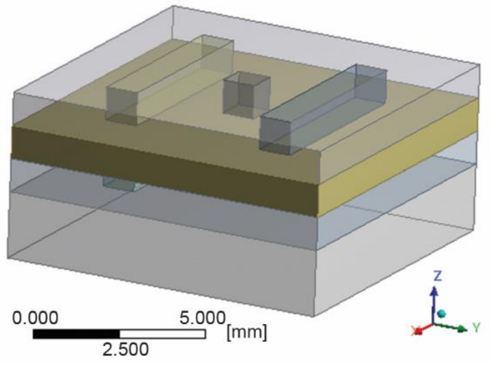

Figure 2. The model of the two-layer 3-D IC

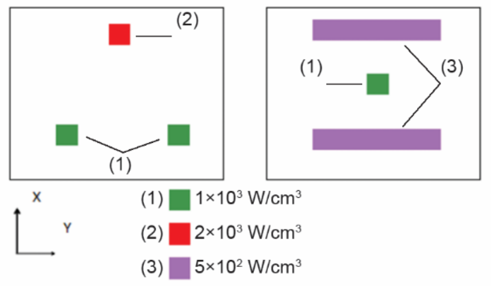

Figure 3. Heat sources distributions of each layer

Experimental results

In this section, a two-layer 3-D IC with different heat source distributions is established to study the temperature fields. By re-arranging the heat source distributions, we get two different heat source distributions to study their effects on the temperature distributions.

The 3-D IC model is shown in fig. 2, where the length and width of each layer are 10 mm, and the heights of the first and second layers are 3 mm and 4 mm, respectively. The thermal properties of layer-1 and layer-2 are listed: the heat conductivity coefficient $k_1 = 50$ W/m°C, $k_2 = 70$ W/m°C, the densities $\rho_1 = 1000$ kg/m^3, $\rho_2 = 2000$ kg/m^3, the specific heat $c_1 = 300$ J/kg°C, $c_2 = 100$ J/kg°C. From the top view of each layer, the heat sources distributions in each layer are shown in fig. 3.

Figure 4 shows the temperature distributions of each layer, where figs. 4(a) and 4(b) represent the temperature fields of the layer-1 and layer-2, respectively. It is obviously that the maximum temperature of layer-1 and layer-2 are 75.732 °C and 76.122 °C, respectively.

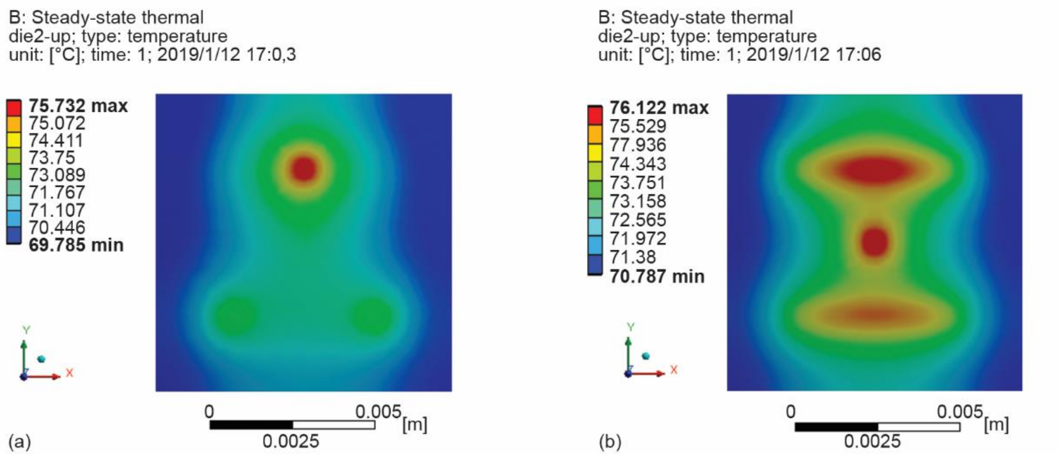

Figure 4. The temperature fields of each layer

For comparison, we consider another case as shown in fig. 5 by rearranging the heat source distributions. In this case, the length and width of each layer are also 10 mm, the heights and thermal properties of the first and second layers are the same as the aforementioned case. The heat sources distributions in each layer are shown in fig. 6.

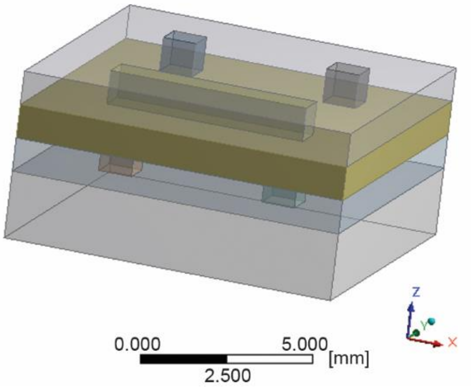

Figure 5. The model of the two-layer 3-D IC

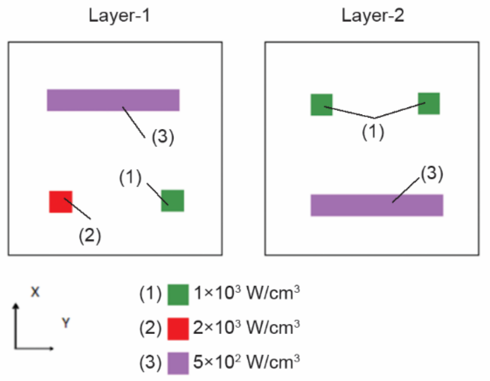

Figure 6. The heat sources distributions of each layer

Figure 7 shows the temperature fields of each layer by rearranging the heat sources distribution, where figs. 7(a) and 7(b) represent the temperature fields of the layer-1 and layer-2, respectively. It is obviously that the maximum temperature of layer-1 and layer-2 are 72.655 °C and 72.507 °C, respectively. By comparing figs. 7 and 4, it can be found that the temperature has been greatly reduced after rearranging the heat sources distribution, where the maximum temperature in layer-1 is reduced by about 4.24% and the maximum temperature in layer-2 is reduced by about 4.99%. The results show that the maximum temperature can be declined by rearranging the heat source distribution.

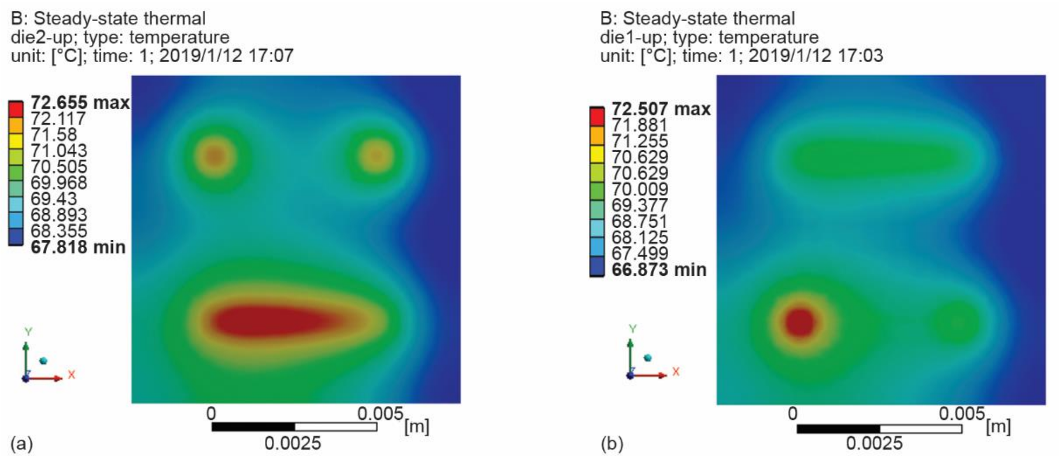

Figure 7. The temperature fields of each layer

Discussions and conclusion

For the steady heat conduction, eq. (2) becomes:

$$k\nabla^2 T + \dot{q} = 0 \tag{3}$$

and a variational-based finite element method can be used, its variational formulation can be established by the semi-inverse method [28-30], which is:

$$J(T) = \iint \left\{ -\frac{1}{2} k (\nabla T)^2 + \dot{q} T \right\} \mathrm{d}x\mathrm{d}y \tag{4}$$

For a micro-scale and nanoscale heat conduction [31], a more accurate model can be established by fractal derivative model [32], and eq. (2) can be updated:

$$C_\mathrm{v} \frac{\mathrm{d}T}{\mathrm{d}t^\alpha} - k \frac{\partial}{\partial x^\beta} \left(k_x \frac{\partial T}{\partial x^\beta} \right) - \frac{\partial}{\partial y^\gamma} \left(k_y \frac{\partial T}{\partial x^\gamma} \right) = \dot{q} \tag{5}$$

where $\mathrm{d}/\mathrm{d}t^\alpha$, $\mathrm{d}/\mathrm{d}x^\beta$, and $\mathrm{d}/\mathrm{d}y^\gamma$ are fractal derivatives with respect to t, x, and y, respectively, α, β, and γ are fractal orders. Detailed discussion of the fractal calculus and its applications are referred to [32-42].

In this paper, the thermal optimization of 3-D IC is studied by rearranging the heat source distribution. The results show that the maximum temperature can be declined by rearranging the heat sources distribution. The results presented in this paper are expected to aid in the development of thermal design guidelines for the 3-D IC.

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