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THERMAL MODEL FOR 3-D INTEGRATED CIRCUITS WITH INTEGRATED MLGNR-BASED THROUGH SILICON VIA

by

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This paper applies the multi-layer graphene nanoribbon as a new prospective filler material for through silicon via to solve the complex heat problems in the 3-D integrated circuits. An equivalent thermal model for 3-D integrated circuits with the MLGNR-based through silicon via is presented in this work, which take lateral heat transfer of through silicon via into account. The experimental results show that the heat transfer performance of MLGNR-based through silicon via is better than the conventional Cu-based through silicon via. Furthermore, it is found that the temperature predicted by the proposed model are in good accordance with the ANSYS simulation, and the maximum relative deviation is less than 4.0%.

Key words: *thermal model, 3-D integrated circuits, MLGNR-based TSV*

Introduction

The 3-D-IC stacking technology is a promising scheme for next generation semiconductor chips, which expand the conventional 2-D integrated circuits (2-D-IC) into a 3-D space by stacking of multiple circuit layers in vertical direction [1-3]. Compared with the 2-D-IC, *N*-die stacked chips can reduce the total wire length, delay, power dissipation and package size [4-6]. However, it is widely recognized that the continuously rising operating frequency and power density of 3-D-IC can cause more and more serious heat problem. Hence, it can be accepted that the thermal management is playing a significant role in solving the heat problems of 3-D-IC [7].

The TSV are integrated in 3-D-IC, which can transfer heat from multiple dies to the heat sink in vertical direction. Thus, TSV are regarded as an effective way to eliminate heat problem in 3-D-IC. In the literature, to date, the Cu is the most common filler material for TSV. However, the excessive temperature rise and high operating frequency can cause the electromigration effect and skin effect of the Cu-based TSV, respectively [8, 9]. Therefore, it is essential to find an alternative to the conventional Cu material for TSV. In the past few years, graphene nanoribbon as an emerging material have attracted intensive research interest on account of its excellent electrical, mechanical and thermal performance [10, 11]. In comparison with Cu, the high quality graphene nanoribbon have large thermal conductivity of 5300 W/mK and current density of 10^9A/cm^2 [10, 12]. According to the number of graphene layers, the graphene nanoribbon can be divided into MLGNR and single-layer grapheme nanoribbon (SLGNR). In

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the light of higher resistivity possess by SLGNR, thus the MLGNR is more suitable to be as potential filler material for TSV [13].

At present, there have been some studies about the performance of MLGNR-based TSV. Hossain *et al.* [14] first proposed the MLGNR as TSV filler material to improve the thermal performance for 3-D-IC, and the experiment results is got by the COMSOL Multiphysics simulation. Goswami *et al.* in [15] presented an equivalent electrical model of MLGNR based TSV, and found that the delay and power dissipation of TSV can be greatly reduced by using MLGNR instead of conventional Cu material. Kumar *et al.* in [16] reviewed the future application prospect of the MLGNR-based TSV for 3-D-IC. In this paper, we propose an analytical thermal model of 3-D-IC with integrated the MLGNR based TSV. In addition, due to the thermal conductivity of TSV is far larger than the device layer, bond layer and silicon substrate, thus our thermal model take the lateral heat transfer into consideration [17]. Compared with the ANSYS simulation, our proposed thermal model can predict the temperature distribution of each die quickly and accurately.

The thermal model of 3-D-IC

The physical structure of 3-D-IC with the integrated MLGNR-based TSV is depicted in fig. 1, where the *N*-die stacked chips are bonded in form of face-to-back.
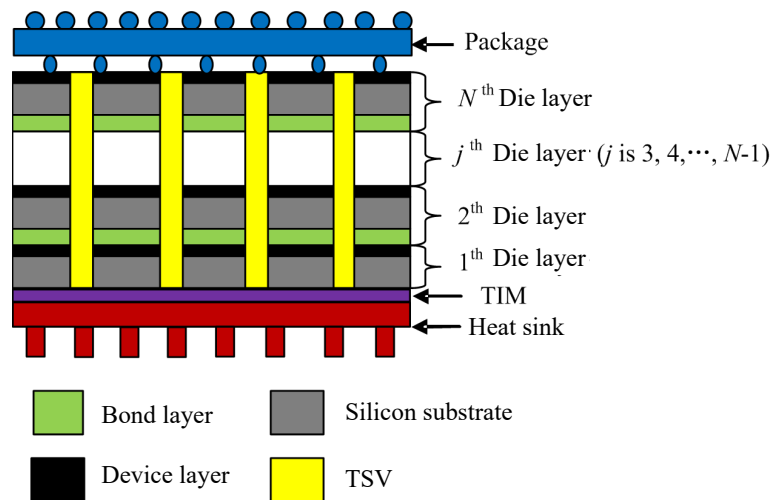

Figure 1. A typical 3-D-IC structure with TSV

It is assumed that the MLGNR-based TSV is uniformly embedded in 3-D-IC, and its top view of geometric configuration is illustrated in fig. 2(a). Here, the *W* and *L* are the width and length of TSV cell for multi-die stack chips, respectively. The cross-sectional view of MLGNR-based TSV is displayed in fig. 2(b), where the l_{gnr} and w_{gnr} are length and width of TSV filler material, respectively. Moreover, the t_{ox} is thickness of isolation dielectric layer (usually SiO_2) of TSV.

In general, for the 3-D-IC without the TSV, the heat generated by the device layer can be transferred from the multiple stacked dies to the ambient through heat sink or the package only in the vertical direction [17, 18]. However, due to thermal conductivity of TSV filler material is far greater than silicon substrate, device layer and bond layer, that is, the heat flow can
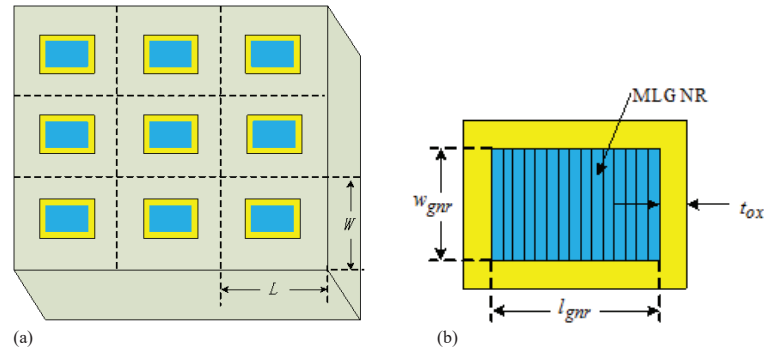
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(a) (b)

Figure 2. The top view of 3-D-IC with the MLGNR-based TSV

be also conveyed from the multiple stacked dies toward the TSV in the lateral direction for the 3-D-IC with the integrated TSV.

Since the overall geometric model is a symmetric structure, as shown in fig. 2(a). Here just part structure (as the $W \times L$ cell structure) is analyzed. Consequently, we develop a 2-D thermal model of MLGNR-based TSV cell to represent the overall thermal model, and its equivalent thermal resistance model is shown in fig. 3. Here, the R_{pk} and R_{hs} are thermal resistance of the package and heat sink, respectively. The $T_{j,a}$ is the temperature of the jth device layer. The $T_{j,c}$ represents the temperature for part of TSV in parallel with the jth device layer, in other words, $T_{j,c}$ is temperature of the jth TSV. The $R_{j,a}$ and $R_{j,c}$ represent the thermal resistance of the jth die layer and the jth TSV, respectively. The $R_{j,b}$ represents the lateral thermal resistance of the jth isolation dielectric layer. The Q_j and T_{amb} are the heat generated from the jth device layer and ambient temperature, respectively.
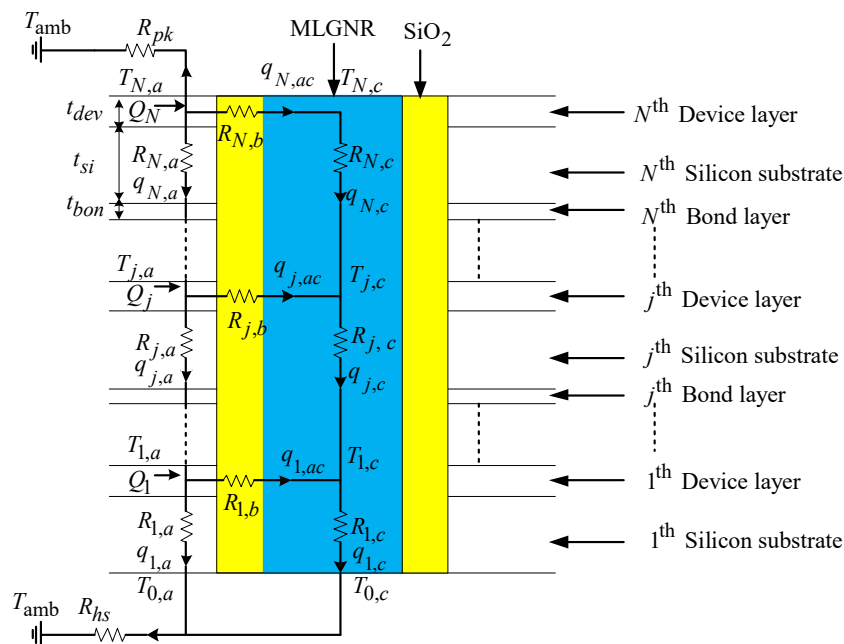

Figure 3. The equivalent thermal resistance model of MLGNR-based TSV cell

The thermal resistance for TSV cell is similar to metal resistance, which can be defined [17,19]:

$$R = \frac{t}{Sk} \tag{1}$$

where the t is thickness of material in vertical direction, the S and k are cross-sectional area of material and thermal conductivity of material respectively. Therefore, the R_{ja}, R_{jb}, and R_{jc} can be written:

$$R_{j,a} = \frac{1}{WL - (l_{gnr} + 2t_{ox})(w_{gnr} + 2t_{ox})} \left(\frac{t_{dev}}{k_{dev}} + \frac{t_{si}}{k_{si}} + \frac{t_{bon}}{k_{bon}} \right) \tag{2}$$

$$R_{j,b} = \int_0^{t_{ox}} \frac{\mathrm{d}x}{2k_{ox}(l_{gnr} + w_{gnr} + 4x)(t_{dev} + t_{si} + t_{bon})} \tag{3}$$

$$R_{j,c} = \frac{t_{dev} + t_{si} + t_{bon}}{l_{gnr} w_{gnr} k_{gnr}} \tag{4}$$

where t_{dev}, t_{si}, and t_{bon} are the thickness of device layer, silicon substrate and bond layer, respectively. The k_{dev}, k_{si}, and k_{bon} are the thermal conductivity of device layer, silicon substrate and bond layer, respectively. The k_{ox} and k_{gnr} are thermal conductivity of isolation dielectric layer and filler material, respectively.

In the steady-state case, the heat flow in all dies can be solved by applying the Kirchhoff's Current Law (KCL). For $j = 1, 2,\ldots\ldots N\text{-}1$, we have:

$$Q_j + q_{j+1,a} = q_{j,a} + q_{j,ac} \tag{5}$$

$$q_{j,ac} + q_{j+1,c} = q_{j,c} \tag{6}$$

where $q_{j,a}$ is the vertical heat flow from the die j to the die j-1, $q_{j,ac}$ represents the lateral heat flow from the die j to the TSV, $q_{j,c}$ – the vertical heat flow of TSV from node j to node $j - 1$. Besides, the relationship between temperature of each die and heat flow can be expressed:

$$T_{j,a} - T_{j-1,a} = R_{j,a} q_{j,a} \tag{7}$$

$$T_{j,a} - T_{j,c} = R_{j,b} q_{j,ac} \tag{8}$$

$$T_{j,c} - T_{j-1,c} = R_{j,c} q_{j,c} \tag{9}$$

Similarly, for $j = 0$, we have:

$$\frac{T_{1,a} - T_{0,a}}{R_{1,a}} + \frac{T_{1,c} - T_{0,c}}{R_{1,c}} = \frac{T_{0,a} - T_{\mathrm{amb}}}{R_{hs}} \tag{10}$$

It is considered that there is the thermal interface materials (TIM) on the heat sink, hence the temperature of TIM can be defined:

$$T_{0,a} = T_{0,c} \tag{11}$$

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For $j = N$, we have:

$$Q_N - \frac{T_{N,a} - T_{\text{amb}}}{R_{pk}} = \frac{T_{N,a} - T_{N-1,a}}{R_{N,a}} + \frac{T_{N,a} - T_{N,c}}{R_{N,b}} \tag{12}$$

$$\frac{T_{N,a} - T_{N,c}}{R_{N,b}} = q_{N,ac} = q_{N,c} = \frac{T_{N,c} - T_{N-1,c}}{R_{N,c}} \tag{13}$$

Equations from (5)-(13) represent $2N+1$ expressions that contain the $2N+1$ variables $T_{N,a}$, $T_{N,c}$, …, $T_{j,a}$, $T_{j,c}$, …, $T_{1,a}$, $T_{1,c}$, $T_{0,a}$. Thus we can obtain the steady-state temperatures of each die by computing the matrix equation:

$$AT = B \tag{14}$$

where A is a $(2N+1) \times (2N+1)$ multi-dimension matrix, where the N denotes the total number of die layer. The element structure of matrix A can be given:

$$A = \begin{bmatrix} \frac{1}{R_{pk}} + \frac{1}{R_{N,a}} + \frac{1}{R_{N,b}} & -\frac{1}{R_{N,b}} & -\frac{1}{R_{N,a}} & 0 & 0 & 0 & 0 & \overset{2N-6}{\overbrace{0...0}} \\ \frac{1}{R_{N,b}} & -\frac{1}{R_{N,b}} - \frac{1}{R_{N,c}} & 0 & \frac{1}{R_{N,c}} & 0 & 0 & 0 & \overset{2N-6}{\overbrace{0...0}} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \overset{2N-2j-2}{\overbrace{0...0}} & -\frac{1}{R_{j+1,a}} & 0 & \frac{1}{R_{j+1,a}} + \frac{1}{R_{j,b}} + \frac{1}{R_{j,a}} & -\frac{1}{R_{j,b}} & -\frac{1}{R_{j,a}} & 0 & \overset{2j-3}{\overbrace{0...0}} \\ \overset{2N-2j-2}{\overbrace{0...0}} & 0 & \frac{1}{R_{j+1,c}} & \frac{1}{R_{j,b}} & -\frac{1}{R_{j,b}} - \frac{1}{R_{j+1,c}} - \frac{1}{R_{j,c}} & 0 & \frac{1}{R_{j,c}} & \overset{2j-3}{\overbrace{0...0}} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \overset{2N-6}{\overbrace{0...0}} & 0 & 0 & 0 & 0 & \frac{1}{R_{1,a}} \frac{1}{R_{1,c}} & -\frac{1}{R_{1,a}} - \frac{1}{R_{1,c}} - \frac{1}{R_{hs}} \end{bmatrix}$$

The B is a $(2N+1) \times 1$ matrix that can be obtained according to the initial conditions and the relevant parameters of the model, and its element structure can be expressed:

$$B = \left[Q_N + \frac{T_{\text{amb}}}{R_{pk}}, \quad 0, \quad \cdots, \quad Q_j, \quad 0, \quad \cdots, \quad -\frac{T_{\text{amb}}}{R_{hs}} \right]^{-1}$$

The T is also a $(2N+1) \times 1$ matrix, which denotes temperature of each die with the element structure as:

$$T = \left[T_{N,a}, \quad T_{N,c}, \quad \cdots \quad T_{j,a}, \quad T_{j,c}, \quad \cdots, \quad T_{0,a} \right]^{-1}$$

It is obviously that the A is a $(2N+1) \times (2N+1)$ sparse matrix, thus the eq. (14) can be efficiently solved by using the sparse matrix solver such as KLU.

Experimental results and discussions

In this section, the models of seven-die stacked chips with the MLGNR-based TSV and Cu-based TSV are investigated by using the proposed method, respectively. In addition, the experimental results are verified with the ANSYS Workbench 15.0 simulations.

Results and discussions of the proposed thermal model

For the convenience of analysis, we assume that the device layer, silicon substrate and bond layer of all dies have the same geometric structure and each device layer generate the same heat, that is , $R_{j,a} = \ldots R_{2,a} = R_{1,a}$, $R_{j,b} = \ldots R_{2,b} = R_{1,b}$, $R_{j,c} = \ldots R_{2,c} = R_{1,c}$, and $Q_j = \ldots Q_2 = Q_1$. Furthermore, the ambient temperature T_{amb} is set to be 28 °C. The physical and geometrical parameters of the model are listed as follows, $W = 40$ μm, $L = 60$ μm, $l_{gnr} = 4$ μm, $w_{gnr} = 2$ μm, $t_{ox} = 0.5$ μm, $t_{dev} = 20$ μm, $t_{si} = 50$ μm, $t_{bon} = 10$ μm, $k_{dev} = k_{ox} = 1.4$ W/mK, $k_{si} = 150$ W/mK, $k_{bon} = 0.15$ W/mK, $k_{gnr} = 2000$ W/mK, $k_{Cu} = 380$ W/mK. The overall chip area S is set to 12 mm × 8 mm, the total thermal resistance of the package and heat sink are named R'_{pk} and R'_{hs}, respectively. Hence the R_{pk} and R_{hs} can be expressed as: $R_{pk} = R'_{pk}S/(WL)$, $R_{hs} = R'_{hs}S/(WL)$, the R'_{pk} and R'_{hs} are equal to 20 K/W and 3 K/W, respectively. Similarly, the total heat generated from each device layer is defined as $Q'_j = 3$ W, so the Q_j can be written as: $Q_j = Q'_jWL/S$. The temperature rise between each die and ambient temperature is defined: $\Delta T_{j,a} = T_{j,a} - T_{amb}$. The temperature results of MLGNR and Cu based TSV cases are shown in Case 1 and Case 2 of tab. 1, respectively. Besides, the temperature rise of each die for MLGNR and Cu based TSV are displayed in tab. 2, respectively.

Table 1. Steady-state temperature of each die for MLGNR and Cu based TSV

	Method	Steady-state temperature of each die layer, $T_{j,a}$ [°C]							
		$j = 7$	$j = 6$	$j = 5$	$j = 4$	$j = 3$	$j = 2$	$j = 1$	$j = 0$
Case 1	Proposed model (MLGNR-based TSV)	42.71	42.80	42.29	41.79	40.93	39.76	38.25	35.41
	ANSYS simulation (MLGNR-based TSV)	43.51	43.48	42.53	41.21	39.67	38.89	37.46	34.18
	Deviation	1.84%	1.56%	0.56%	1.41%	3.18%	2.24%	2.11%	3.60%
Case 2	Proposed model (Cu-based TSV)	62.42	62.89	59.85	56.69	53.41	49.03	43.53	36.91
	ANSYS simulation (Cu-based TSV)	63.16	63.21	59.01	56.86	52.01	48.18	41.87	35.56
	Deviation	1.17%	0.51%	1.42%	0.29%	2.69%	1.76%	3.96%	3.79%

Table 2. Temperature rise of each die for MLGNR and Cu based TSV

Method	Temperature rise of each die layer, $\Delta T_{j,a}$ [°C]							
	$j = 7$	$j = 6$	$j = 5$	$j = 4$	$j = 3$	$j = 2$	$j = 1$	$j = 0$
Proposed model (MLGNR-based TSV)	14.71	14.80	14.29	13.79	12.93	11.76	10.25	7.41
Proposed model (Cu-based TSV)	34.42	34.89	31.85	28.69	25.41	21.03	15.53	8.91

As is shown in tab. 1, it can be observed that the steady-state temperature of MLGNR-based TSV case is lesser than Cu-based TSV scheme at all die layer. As an instance, for the $j = 6$ die layer, the steady-state temperature in the MLGNR-based TSV case reduces by 31.94% compared with Cu-based TSV scheme. The reason for this phenomenon is that the thermal conductivity of MLGNR is far larger than the conventional Cu material. As a consequence,

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under the MLGNR-based TSV cases, there is a greater proportion of the lateral heat transfer toward TSV than Cu-based TSV scheme. In addition, the experimental results obtained by the proposed model match closely enough with ANSYS simulation, where the maximum relative deviation for MLGNR-based TSV and Cu-based TSV cases are 3.60% and 3.96%, respectively.

According to the tab. 2, it is shown that the MLGNR-based TSV case has lesser temperature rise than the traditional Cu-based TSV scheme at any die layer. For example, the maximum temperature rise of Cu-based TSV case is 19.71 °C higher than the MLGNR-based scheme at the $j = 7$ die layer. Hence, it indicates that the MLGNR can be used as the potential alternative material of TSV to replace Cu.

In order to investigate the relationship between temperature rise of each die and the size of TSV. Here, the area ratio of TSV is defined as: $A_r = (l_{gnr} + 2t_{ox})(w_{gnr} + 2t_{ox})/(WL)$. The temperature rise of each die with different area ratio of MLGNR and Cu based TSV are plotted in fig. 4, respectively.

As is shown in fig. 4, it is obvious that the temperature rise will be decreased with the increasing of area ratio for both Cu and MLGNR based TSV cases. For instance, when the area ratio of TSV increases from 0.005 to 0.04, the percentage reduction of temperature rise is 35.28% for MLGNR-based TSV case and 54.53% for Cu-based TSV scheme at the $j = 7$

Figure 4. Temperature rise of each die with different area ratio of TSV

die layer. The reason for this situation is that the proportion of heat transmission through TSV in the lateral direction will increase as the size of TSV increases. Meanwhile, the declines of temperature rise are no longer obvious when the area ratio of TSV increases to a certain value. Therefore, it is essential that the chip designer ought to choose a reasonable size of TSV. This is due to the oversize TSV will take up the chip space.
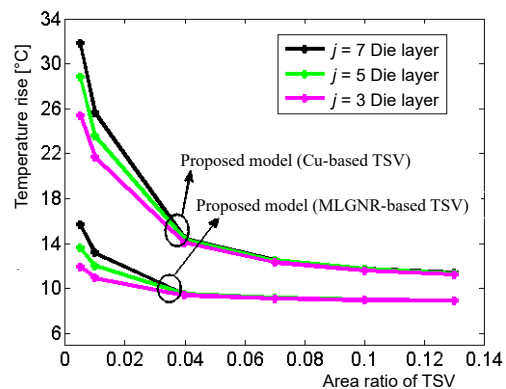
Results of ANSYS simulation

In order to verify the accuracy of our proposed method, the ANSYS Workbench 15.0 as a finite element analysis simulation tool is used to obtain the steady-state temperatures of each die layer. Herein, due to the symmetry of the geometric structure, just part structure (as the $W \times L$ cell structure) is investigated. We use the DesignModeler of ANSYS Workbench 15.0 to built a seven-die stacked chips with the TSV (MLGNR based TSV or Cu based TSV), as shown in the fig. 5. Similarly, it is observed from the figure that the cell structure includes TSV, heat sink, package, silicon layer, device layer and bond layer. Next, the relevance center and smoothing of mesh parameters are set as the fine and high, respectively. The corresponding mesh structure is depicted in fig. 6, where there are a total of 28325 nodes and 9415 elements.

The steady-state temperatures of each die layer are solved by running the mechanical APDL solver of ANSYS Workbench. The environment of this solver is defined as internal heat generation, which are added in each device layer. By performing the mechanical APDL solver, the temperature distribution of MLGNR based TSV and Cu based TSV schemes are described in figs. 7(a) and 7(b), respectively. In addition, we can apply the Probe Tool of ANSYS Workbench to obtain the accurate steady-state temperatures of each die layer. The temperature results of ANSYS simulation for MLGNR based TSV and Cu based TSV schemes are shown
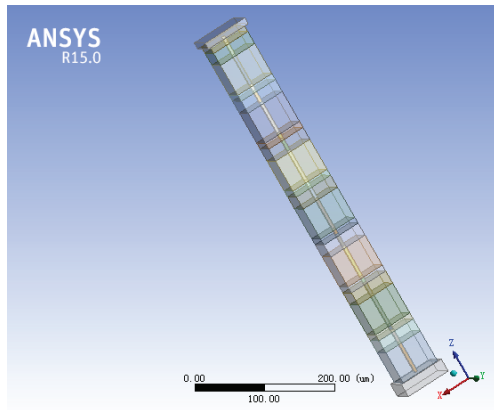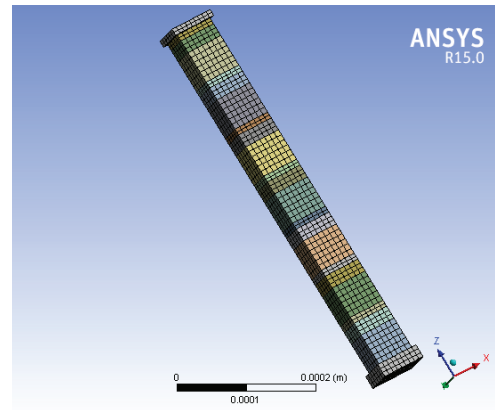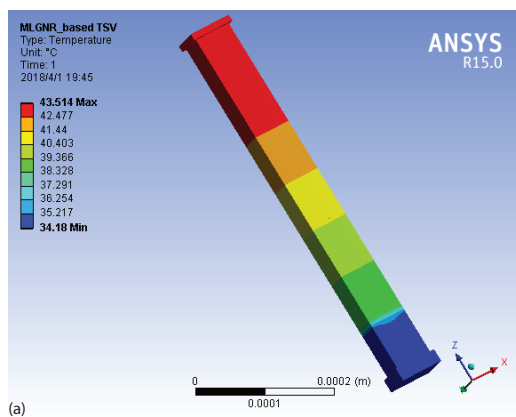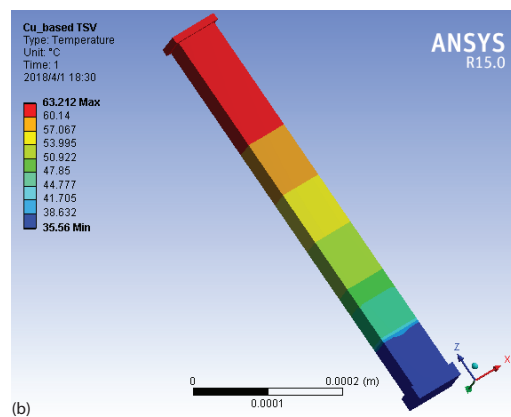
Figure 5. The geometry model with the TSV

Figure 6. The mesh model with the TSV

Figure 7. The temperature distribution; (a) MLGNR based TSV scheme and (b) Cu based TSV scheme

in Case 1 and Case 2 of tab. 1, respectively. The relative deviation of tab. 1 is defined as: (|temperature of ANSYS simulation – temperature of proposed model|)/temperature of ANSYS simulation.

Based on the previous comparisons of experimental results, it is shown that the results obtained by the proposed model in the paper have close agreement with the ANSYS simulations. Moreover, the MLGNR can be applied as a new prospective filler material of TSV if the thermal management is taken as the main consideration in the design of 3-D-IC. And it is vital to find the suitable size of TSV in 3-D-IC.

Conclusion

The paper presents an equivalent thermal model of 3-D-IC with integrated MLGNR-based TSV, which take the lateral thermal resistance into consideration. The experimental results show that the MLGNR-based TSV can reduce the chip temperature more effectively compared with the conventional Cu-based TSV. Therefore, the MLGNR as a new emerging filler material for TSV has a better application prospect in the 3-D-IC. In addition, it is found that choosing an appropriate size of TSV is very important for the 3-D-IC designer. Furthermore, the results obtained by the proposed approach in this paper have great consistency with the ANSYS sim-

ulations. Consequently, in view of the current research progress, the proposed thermal model may be helpful in solving the complex thermal management of 3-D-IC in the future.

Acknowledgment

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