# ANALYTICAL THERMAL MODELLING OF MULTILAYERED ACTIVE EMBEDDED CHIPS INTO HIGH DENSITY ELECTRONIC BOARD

by

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*The recent printed wiring board embedding technology is an attractive packaging alternative that allows a very high degree of miniaturization by stacking multiple layers of embedded chips.*
*This disruptive technology will further increase the thermal management challenges by concentrating heat dissipation at the heart of the organic substrate structure.*
*In order to allow the electronic designer to early analyse the limits of the power dissipation, depending on the embedded chip location inside the board, as well as the thermal interactions with other buried chips or surface mounted electronic components, an analytical thermal modelling approach was established.*
*The presented work describes the comparison of the analytical model results with the numerical models of various embedded chips configurations. The thermal behaviour predictions of the analytical model, found to be within ±10% of relative error, demonstrate its relevance for modelling high density electronic board.*
*Besides the approach promotes a practical solution to study the potential gain to conduct a part of heat flow from the components towards a set of localized cooled board pads.*

Key words: *thermal modelling, electronic board cooling, embedded active chip*

## Introduction

Continuous trend towards electronics miniaturization to answer the strong need to execute more functions in less space, has drastically affected the stakes of the electronic design.

The great technological capabilities of board chip embedding for electronic systems were highlighted by the European "Hiding Dies" and "HERMES" projects.

The main objective was to develop the concept of embedded thin active chips at the heart of a printed wiring board (PWB) structure as a base for an integrated electronic circuits manufacturing. The construction process consists in burying thin chips inside laminated build-up layers, so called core layers, then integrating them between conventional multilayered substrates.

The aim of the following analytical modelling approach is to determine the temperature distribution of the embedded chips and to assess the impact of external surface mounted devices (SMD) on them, at laboratory conditions.

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## Analytical model for single core layer

This part focuses on the steady-state thermal analysis of a mono chip which is buried in a single core layer. The electronic board is considered cooled by coupled convection and radiation heat exchanges.

The board shape can be approximated by a parallelepiped and its multilayered structure replaced by two orthotropic layers in perfect thermal contact. Their respective thickness depends on the location of the internal heating source of the buried chip.

Like in many conventional studies on PWB thermal behaviour, the four lateral edges are assumed to be adiabatic due to their very thin thickness. Thus the heat of chip is only removed through upper and lower surfaces. Each of these surfaces is submitted to a specific uniform heat transfer coefficient according to the Newton's law, named respectively ht and hr. Those ones combine convection and radiation effects and allow us to take into account the gravity orientation.

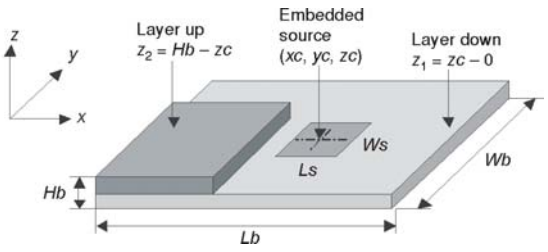


**Figure 1. Definition of geometric parameters of the analytical model**

The board length, width, and thickness are defined, respectively, by *Lb*, *Wb* and *Hb* as pictured in fig. 1.

The set of equations describing the proposed model and its boundary conditions are summarized below.

Generalized governing equation depending on a set of axial thermal conductivity values, defined *kx*, *ky* or *kz*:

$$kx_i \frac{\partial^2 \theta_i(x, y, z)}{\partial x^2} + ky_i \frac{\partial^2 \theta_i(x, y, z)}{\partial y^2} + kz_i \frac{\partial^2 \theta_i(x, y, z)}{\partial z^2} = 0 \quad \text{for} \quad i = 1, Nl \tag{1}$$

External boundary conditions for $0 \le x \le Lb$ and $0 \le y \le Wb$:

$$kx_i \frac{\delta \theta_i(x, y, z)}{\delta x^2}\bigg|_{x=0,Lb} = 0 \quad \text{and} \quad ky_i \frac{\delta \theta_i(x, y, z)}{\delta y}\bigg|_{y=0,Wb} = 0 \quad \text{for} \quad i = 1, Nl \tag{2}$$

$$-kz_{Nl} \frac{\delta \theta_{Nl}(x, y, z)}{\delta z}\bigg|_{z=Hb} = ht\theta_{Nl}(x, y, z) \quad \text{and} \quad -kz_1 \frac{\delta \theta_1(x, y, z)}{\delta z}\bigg|_{z=0} = -hr\theta_1(x, y, z) \tag{3}$$

Interlayer temperature and flux continuity boundary conditions, for $0 \le x \le Lb$ and $0 \le y \le Wb$:

$$\theta_{i+1}(x, y, z)\big|_{z=z_i} = \theta_i(x, y, z)\big|_{z=z_i} \quad \text{for} \quad i = 1, Nl - 1 \tag{4}$$

$$kz_{i+1} \frac{\delta \theta_{i+1}(x, y, z)}{\delta z}\bigg|_{z=z_i} - kz_i \frac{\delta \theta_i(x, y, z)}{\delta z}\bigg|_{z=z_i} = E(x, y) \quad \text{for} \quad i = 1, Nl - 1 \tag{5}$$

The 3-D temperature distribution of an embedded chip in a PWB has been solved using conventional Fourier series [1-3] but other techniques are pertinent as well [4]. Some other analytical solutions applied to the diffusion of heat have been suggested in the literature [5-8].

A final solution of the temperature distribution can be written as:

$$\theta_i(x, y, z) = \frac{q}{LsWs} \sum_{m=1}^{M} \sum_{n=1}^{N} A_m B_n \cos\left(\frac{m\pi}{Lb} x\right) \cos\left(\frac{n\pi}{Wb} y\right) \omega e_{m,n,i}(z) \tag{6}$$

where the relationships of the Fourier coefficient $A_{\mathrm{m}}$ and $B_{\mathrm{n}}$ are:

$$A_m = 4 \frac{\sin\left(\frac{m\pi}{Lb}\frac{Ls}{2}\right)\cos\left(\frac{m\pi}{Lb} xc\right)}{m\pi + \delta_m} + \frac{Ls}{Lb}\delta_m \tag{7a}$$

$$B_n = 4 \frac{\sin\left(\frac{n\pi}{Wb}\frac{Ws}{2}\right)\cos\left(\frac{n\pi}{Wb} yc\right)}{n\pi + \delta_n} + \frac{Ws}{Wb}\delta_n \tag{7b}$$

The source length, width and its center location are defined, respectively, by *Ls*, *Ws*, *xc*, and *yc*. The Kronecker function $\delta$ is brought to extend formulae validity to the cases where *m* and/or *n* are equal to zero.

The z-axis thermal profile, $\omega e_{m,n,i}(z)$, over the cross-section is depending on the number of layers which are to be scrutinized to characterize the board thermal behavior, in our case two juxtaposed layers:

$$0 \le z \le zc \Rightarrow \ \omega e_{m,n,1}(z) = \frac{D_{m,n,1}}{E_{m,n,1}} \left[\frac{\chi u_1}{kz_1}\gamma(r_{m,n,1}, z) + ch(r_{m,n,1} z)\right] \text{ with } \chi u_1 = hr \tag{8}$$

$$zc \le z \le Hb \Rightarrow \ \omega e_{m,n,2}(z) = \frac{1}{E_{m,n,1}} \left[\frac{\chi l_1}{kz_2}\gamma(r_{m,n,2}, z) + ch(r_{m,n,2} z)\right] \tag{9a}$$

with

$$\chi l_2 = -\frac{kz_2 (r_{m,n,2})^2 \gamma(r_{m,n,2}, Hb) + htch(r_{m,n,2} Hb)}{ch(r_{m,n,2} Hb) + \frac{ht}{kz_2}\gamma(r_{m,n,2}, Hb)} \tag{9b}$$

Finally, all parameters of the solution are given by:

$$D_{m,n,i} = \frac{\frac{\chi l_{i+1}}{kz_{i+1}}\gamma(r_{m,n,i+1}, zc_i) + ch(r_{m,n,i+1} zc_i)}{\frac{\chi u_i}{kz_i}\gamma(r_{m,n,i}, zc_i) + ch(r_{m,n,i} zc_i)} \tag{10}$$

$$\begin{aligned} E_{m,n,i} = {} & D_{m,n,i}[\chi u_i ch(r_{m,n,i} zc_i) + kz_i (r_{m,n,i})^2 \gamma(r_{m,n,i}, zc_i)] - \\ & -[\chi l_{i+1} ch(r_{m,n,i+1} zc_i) + kz_{i+1} (r_{m,n,i+1})^2 \gamma(r_{m,n,i+1}, zc_i)] \end{aligned} \tag{11}$$

$$r_{m,n,i} = \sqrt{\frac{kx_i}{kz_i}\left(\frac{m\pi}{Lb}\right)^2 + \frac{ky_i}{kz_i}\left(\frac{n\pi}{Wb}\right)^2} \tag{12}$$

$$\gamma(r_{m,n,i}, z) = \frac{sh(r_{m,n,i}, z)}{r_{m,n,i} + \delta_n \delta_m} + z\delta_n \delta_m \tag{13}$$

Electronic PWB are complex multi-layered structures in which high thermal conductivity of copper layers are sandwiched between low thermal conductivity of glass-epoxy layers.

Thus the effective thermal conductivity of that stack-up is anisotropic with a high heat spreading capability along the PWB XY-plane.Thus assumed effective thermal conductivities and thicknesses of both homogenous blocks, at a location corresponding to the heating surface of the chip are defined (in tab. 1).

**Table 1. Effective thermal conductivities of both layers**

| Layer | Index | $\Sigma t_l$ | $kx_i$ and $ky_i$ | $kz_i$ |
|---|---|---|---|---|
| $t_2 \le z \le H_b$ | 1 | 0.43 mm | 46 W/mK | 1.17 W/mK |
| $0 \le z \le t_2$ | 2 | 0.7 mm | 28.7 W/mK | 1.17 W/mK |

The remaining work consists in establishing the relationships that will allow to characterize heat transfer coefficients to apply on board's top ($z = 0$) and rear ($z = Hb$) surfaces, respectively, named ht and hr.

## Equivalent heat transfer coefficient calculation

In practice, to estimate the surface temperatures of an electronic board, which is assimilated to a flat plate in unlimited space, empirical correlations [9-14] are considering a set of dimensionless numbers, such as known Grashoff (Gr) Prandtl (Pr) or Rayleigh (Ra).

Lewandowki and Kubski [15] conducted a fine investigation with the purpose of establishing a final set of relationships dedicated to vertical and horizontal plates. This one demonstrates that the correlation is strongly influenced by the characteristic length, or $\mathcal{L}$, which is connected with the geometry of the heating plate and its definition turns out to be an issue.

Nevertheless, Yovanovich [16] and Yovanovich and Jafarpur [17] established a revised definition of characteristic length by using the square root of the total active surface area, $\mathcal{L} = S^{1/2}$.

Furthermore the relationship of the characteristic length considers all dimensions of the board with $\alpha = 1$:

$$\mathcal{L} = \sqrt{Sb} = \sqrt{LbWb + \alpha Hb(Lb + Wb)} \tag{14}$$

Thus a general expression for natural convection heat transfer coefficient from isothermal 3-D bodies was proposed in the form for horizontal plate with both active sides:

$$ht \text{ or } hr = \frac{k_a}{\mathcal{L}} \left\{ 0.67 \left[ 1 + \left( \frac{0.5}{\mathrm{Pr}} \right)^{9/16} \right]^{-4/9} \right\} \left[ 0.7 \left( 2\frac{Lb}{Wb} \right)^{1/8} \right] (\mathrm{Ra}_{\mathcal{L}})^n$$

$$\text{or } \frac{k_a}{\mathcal{L}} C(\mathrm{Ra}_{\mathcal{L}})^n \text{ or } \frac{k_a}{\mathcal{L}} C(\mathrm{Gr}_{\mathcal{L}}\,\mathrm{Pr})^n \tag{15}$$

Finally, the heat transfer coefficient is summed with a radiative heat exchange expression depending on emissivity $\varepsilon$ and radiative surface configuration factor $F$ as well as surface and ambient absolute temperature:

$$h_f = \frac{k_a}{\mathcal{L}} C_f (\mathrm{Ra}_{\mathcal{L}})^n + \varepsilon_f \sigma F_{f\to\infty} S_f (\breve{T}_f^2 + \breve{T}_\infty^2)(\breve{T}_f + \breve{T}_\infty) \tag{16}$$

Thus, the equivalent heat transfer coefficient ($h_f$) is correlated with upper and rear board environment.

## Calculation corner

Mathcad® software was used to run the analytical model calculations, defined in the various result tables by the subscript M, for mathematical approach.

The computational fluid dynamics software, Icepak® and Flotherm®, were selected to generate the board lumped or fine realistic models as well as to compute the environment conditions such as conjugated free convection and radiation. These models are designated by the subscript N for numerical computation.

## Thermal behavior of a single buried chip

The dimensions of the studied board are $Lb = 100$ mm, $Wb = 160$ mm, and $Hb = 1.13$ mm.

The first analysis focuses on the thermal behaviour of a single source and a fixed uniform equivalent heat transfer coefficient of 10 W/m$^2$K is applied on the board's top and rear external surfaces. This unfounded value is commonly assigned to characterise free convection combined with radiation.

The comparison is done on the central temperature ($xc$, $yc$, $zc$) of the source and its mean temperature:

$$\overline{\theta}_i(xc, Ls, yc, Ws, zc) = \sum_{m=1}^{M}\sum_{n=1}^{N}\frac{q}{LsWs}A_m B_n \overline{A_m}\,\overline{B_n}\omega e_{m,n,i}(z) \tag{17}$$

where the average Fourier coefficients are given by:

$$\overline{A_m}\,\overline{B_n} = \left[2\frac{Lb}{Ls}\frac{\sin\left(\frac{m\pi}{Lb}\frac{Ls}{2}\right)\cos\left(\frac{m\pi}{Lb}xc\right)}{m\pi+\delta_m}+\delta_m\right]\left[2\frac{Ws}{Wb}\frac{\sin\left(\frac{n\pi}{Wb}\frac{Ws}{2}\right)\cos\left(\frac{n\pi}{Wb}yc\right)}{n\pi+\delta_n}+\delta_n\right] \tag{18}$$

Table 2 declines some cases which compare the predictions of the analytical approach (M) to those of a numerical model (N). A specific error metric, named $\Delta T_S = (T_M - T_N)/(T_N - T_A)$ expressed as a percentage, compares the analytical calculation with the numerical result considering it as the reference value:

**Table 2. Temperature predictions of single embedded source**

| | | | | | | | M. model | | N. model | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Case | $xc$ | $yc$ | $L_S$ | $W_S$ | $Q_S$ | $T_A$ | $\overline{T}_M$ | $T_M$ | $\overline{T}_N$ | $T_N$ | $\overline{\Delta T}_S$ | $\Delta T_S$ |
| | [mm] | [mm] | [mm] | [mm] | [W] | [°C] | [°C] | [°C] | [°C] | [°C] | [%] | [%] |
| 1 | 50 | 80 | 7 | 7 | 1.5 | 85 | 105.2 | 107.1 | 105.2 | 106.8 | 0.4 | 1.4 |
| 2 | 50 | 80 | 7 | 7 | 1.5 | 20 | 40.2 | 42.1 | 40.2 | 41.8 | 0.3 | 1.4 |
| 3 | 50 | 80 | 10 | 7 | 1.5 | 35 | 53.5 | 55.3 | 53.4 | 55.0 | 0.6 | 1.7 |

* $ht = hr = 10$ W/m$^2$K

The results agreement for various scenario demonstrates that the stated approach is suitable to analyse the thermal behaviour of buried single source.

Further, the pertinence of the analytical model has to be check for realistic environment conditions when heat transfers depend on the board temperature distribution as well as air moving phenomena.

Considering the boundary conditions of the case 1, tab. 3 presents the comparison of the proposed analytical calculation (M) of the equivalent heat transfer coefficient to the values provided by the numerical model (N) when air moving phenomena and radiation effect are computed with a board emissivity of 0.95.

The comparison of the convective heat transfer coefficients highlights the poor agreement of the analytical approach to the numerical results.

**Table 3. Board's heat transfer coefficients evaluation**

| | | Equivalent | | Convective | | Radiative | |
|---|---|---|---|---|---|---|---|
| Gravity axis | Model | Top | Rear | Top | Rear | Top | Rear |
| g = –*z* | M | 12.2 | 12.2 | 2.1 | 2.1 | 10.1 | 10.1 |
| | N | 11.9 | 11.8 | 1.78 | 1.68 | 10.1 | 10.1 |

* In $Wm^2K$

Nevertheless, the radiative exchange drives the chip heat transfer, so the divergence between the centre and mean temperatures of the chip is less than 1%, which is our primary concern. Moreover, the average temperatures of the board in both models are concurring.

The comparison of results, this time with "realistic" boundary conditions, are resumed in tab. 4

**Table 4. Revised chip temperature predictions of single embedded source**

| Case 1 | M. model | | N. model | | | |
|---|---|---|---|---|---|---|
| Gravity axis | $\overline{T}_M$ | $T_M$ | $\overline{T}_N$ | $T_N$ | $\overline{\Delta T}_S$ | $\Delta T_S$ |
| | [°C] | [°C] | [°C] | [°C] | [%] | [%] |
| g = –*z* | 104.2 | 106.1 | 104.1 | 105.9 | –0.3 | –0.8 |

## Extension for multiple buried sources

For a set of buried chips, the solution for the temperature distribution may be obtained using the superposition principle. Then for N heating sources, the 3-D temperature distribution is:

$$T_i(x, y, z) - T_A = \sum_{s=1}^{Ns} Q_S \sum_{m=1}^{M} \sum_{n=1}^{N} A_{m,s} B_{n,s} \cos\left(\frac{m\pi}{Lb} x\right) \cos\left(\frac{n\pi}{Wb} y\right) \omega e_{m,n,i}(z) \tag{19}$$

Two new chips, named C2 and C3, are taken into account in the analysis of the thermal behaviour of the "two homogenous layers" board model. The heating sources of both chips are localized at the previous board height.

Table 5 displays the predictions of the proposed analytical approach (M) to those of a numerical model (N).

**Table 5. Temperature predictions of three embedded sources**

| | | | | | | | M. model | | N. model | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Gravity axis | Chip | *xc* | *yc* | $L_S$ | $W_S$ | $Q_S$ | $\overline{T}_M$ | $T_M$ | $\overline{T}_N$ | $T_N$ | $\overline{\Delta T}_S$ | $\Delta T_S$ |
| | | [mm] | [mm] | [mm] | [mm] | [W] | [°C] | [°C] | [°C] | [°C] | [%] | [%] |
| –z | C1 | 50 | 80 | 7 | 7 | 2 | 120.3 | 122.9 | 120.2 | 122.6 | –0.3 | –0.7 |
| | C2 | 50 | 110 | 7 | 7 | 1.5 | 125.7 | 127.6 | 125.3 | 127.1 | –0.9 | –1.1 |
| | C3 | 58 | 110 | 7 | 7 | 2 | 128.1 | 130.7 | 127.7 | 130.1 | –1.0 | –1.3 |

* $T_A$ = 85 °C

The analytical model discrepancy stays below 2% and demonstrates its capability for modelling the thermal interactions of a set of buried chips. Furthermore, all industrial PWB have their outer surfaces overpopulated by electronic components that have a significant impact on board temperature profile.

## Board upper and lower sources modelling

To determine the influence of heating devices on the upper and rear surfaces of the PWB, the conventional 3-D temperature distribution for two-layered substrate is solved for a new set of boundary conditions.

Updated interlayer flux boundary condition for $0 \le x \le Lb$ and $0 \le y \le Wb$, eq. (20):

$$kz_{i+1}\left.\frac{\delta\theta_{i+1}(x,y,z)}{\delta z}\right|_{z=z_i} - kz_i\left.\frac{\delta\theta_i(x,y,z)}{\delta z}\right|_{z=z_i} = 0 \quad \text{for} \quad i = 1, Nl-1 \tag{20}$$

Revised substrate's upper and rear surfaces boundary conditions for $0 \le x \le Lb$ and $0 \le y \le Wb$, when a heating source is on upper surface eq. (21) or on rear surface eq. (22):

$$-kz_{Nl}\left.\frac{\delta\theta_{Nl}(x,y,z)}{\delta z}\right|_{z=Hb} = ht\theta_{Nl}(x,y,z) - U(x,y) \quad \text{with} \quad Nl = 2 \tag{21}$$

$$-kz_1\left.\frac{\delta\theta_1(x,y,z)}{\delta z}\right|_{z=0} = -hr\theta_1(x,y,z) + L(x,y) \tag{22}$$

The final solution form of the temperature distribution is quite similar to previous established expression:

$$\theta_i(x,y,z) = \sum_{s=1}^{Ns} Q_s \sum_{m=1}^{M}\sum_{n=1}^{N} A_{m,s}B_{n,s}\cos\left(\frac{m\pi}{Lb}x\right)\cos\left(\frac{n\pi}{Wb}y\right)Z_{m,n,s,i}(z) \tag{23}$$

Hence depending on component location, the right z-axis relationship is selected, using Kronecker function:

$$Z_{m,n,s,i}(z) = \delta(zc_s)\omega r_{m,n,i}(z) + \delta(t_2 - zc_s)\omega e_{m,n,i}(z) + \delta(Hb - zc_s)\omega u_{m,n,i}(z) \tag{24}$$

The complete expressions of $\omega u_{m,n,i}(z)$ and $\omega r_{m,n,i}(z)$ are provided in the Appendix.

## Component boundary conditions modelling

In order to estimate the critical temperature of a SMD, as called junction, the linear compact thermal model (CTM) concept proposed by European DELPHI consortium is exploited.

So the component temperature determination can be summarized by two heat spreading paths in parallel that link its junction (J) to the reference temperature, as shown in fig. 2.

To reach this purpose, the component heat transfer paths to its surrounding have to be characterized.

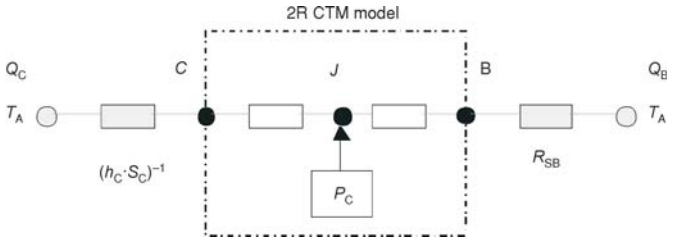


**Figure 2. Definition of elementary heat paths of electronic component**

Thus the thermal spreading resistance of a heating source on a substrate, named Source to Board, is given by:

$$RSB_j(xc_j, yc_j, zc_j \Rightarrow i) = \frac{1}{Q_j}\sum_{s=1}^{Ns} Q_s \sum_{m=1}^{M}\sum_{n=1}^{N} A_{m,s}B_{n,s}\cos\left(\frac{m\pi}{Lb}x\right)\cos\left(\frac{n\pi}{Wb}y\right)Z_{m,n,s,i}(z) \quad (25)$$

The convective heat transfer is defined by a set of body gravity functions for isothermal cuboids mounted on a plate, proposed by Yovanovich and Jafarpur, depending on the characteristic length, eq. (14), with $\alpha = 2$.

Device on upper surface of an horizontal plate:

$$G_{\mathcal{L}} = \frac{[(2^{1/6})(Lc^{4/3}Wc) + (2^{4/3}Hc)(Lc+Wc)^{4/3}]}{[LcWc + 2Hc(Lc+Wc)]^{7/8}} \quad (26)$$

Device on rear surface of an horizontal plate:

$$G_{\mathcal{L}} = \frac{[(2^{-7/6}Lc^{4/3}Wc) + (2^{4/3}Hc)(Lc+Wc)^{4/3}]^{3/4}}{[LcWc + 2Hc(Lc+Wc)]^{7/8}} \quad (27)$$

## Compact thermal modelling of electronic component

Two plastic components called MLF64 and MLF32 are simulated as a CTM network on the upper and rear surface. Their deducted behavioral model was limited to triangle network form and two external surfaces in order to simplify the understanding of the proposed approach. So three nodes, called junction (J), top (Case or C) and bottom (Board or B), were kept and linked by three thermal resistors. The heating power of the component is attached to the junction node (tab. 6).

**Table 6. MLF64 and MLF32 thermal behavioral models**

| CTM | $R_{J\text{-}B}$ | $R_{J\text{-}C}$ | $R_{B\text{-}C}$ | Case surface $S_C$ | Board area $S_B$ |
|---|---|---|---|---|---|
| | [KW$^{-1}$] | [KW$^{-1}$] | [KW$^{-1}$] | [mm$^2$] | [mm$^2$] |
| MLF64 | 3.4 | 56.8 | 14 | 9 × 9 + 4(9 × 0.9) | 9 × 9 |
| MLF32 | 7.9 | 140 | 47.7 | 5 × 5 + 4(5 × 0.9) | 5 × 5 |

The specific board thermal behaviour taking into account multiple kind of heating sources is displayed in tab. 7 for a global power consumption of 3.1 W, at an ambient temperature of 85 °C.

**Table 7. Board temperature predictions of mixed sources**

| | | | | | | | | M. model | | N. model | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Gravity y axis | Device | *xc* | *yc* | *zc* | $L_S$ | $W_S$ | $Q_S$ | $\overline{T}_M$ | $T_M$ | $\overline{T}_N$ | $T_N$ | $\overline{\Delta T}_S$ | $\Delta T_S$ |
| | | [mm] | [mm] | [mm] | [mm] | [mm] | [W] | [°C] | [°C] | [°C] | [°C] | [%] | [%] |
| –*z* | C1 | 50 | 80 | $t_2$ | 7 | 7 | 0.45 | 103.4 | 104.4 | 103.9 | 104.8 | 2.3 | 1.9 |
| | C2 | 50 | 110 | $t_2$ | 7 | 7 | 0.8 | 107.3 | 108.3 | 107.5 | 108.5 | 0.7 | 0.5 |
| | C3 | 58 | 110 | $t_2$ | 7 | 7 | 0.6 | 108.1 | 109.5 | 108.3 | 109.5 | 0.7 | –0.2 |

In addition, the network temperatures and heat flow rates are resumed in tab. 8

**Table 8. Thermal behavior prediction of surface mounted components**

| | | | | | | M. model | | | | N. model | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Gravity axis | Device | *Lc* | *Wc* | *Hc* | *Pc* | $T_{J\text{-}M}$ | $T_{C\text{-}M}$ | $Q_C$ | $Q_B$ | $T_{J\text{-}N}$ | $T_{C\text{-}N}$ | $Q_C$ | $Q_B$ | $\Delta T_J$ |
| | | [mm] | [mm] | [mm] | [W] | [°C] | [°C] | W | W | [°C] | [°C] | [W] | [W] | [%] |
| –z | MLF64 | 9 | 9 | 0.9 | 0.75 | 109.0 | 106.6 | 0.041 | 0.709 | 108.9 | 106.5 | 0.0464 | 0.701 | –0.1 |
| | MLF32 | 5 | 5 | 0.9 | 0.5 | 116.0 | 112.3 | 0.025 | 0.475 | 114.5 | 111.0 | 0.0191 | 0.476 | –5.4 |

The temperature and heat flow rate agreements, better than 10%, prove that the developed approach is an efficient tool to investigate several design options at early stage of a project, our initial prospect.

## Extension of cooling boundary conditions

The approach can be completed to investigate the potential gain to drain a significant part of the heat to a set of cooled board pads. Thus the average temperature of a peculiar cooling local area (*d*) is given by:

$$\overline{Td_{i,j}}(xcd_j, Ld_j, ycd_j, Wd_j, zcd_j) - T_\infty = \sum_{s=1}^{Ns} \overline{R}_{CB_{i,s}}(xcd_j, Ld_j, ycd_j, Wd_j, zcd_j) q_s + \\ + \sum_{d=1}^{Nd} \overline{R}_{FB_{i,d}}(xcd_j, Ld_j, ycd_j, Wd_j, zcd_j) - qf_d \quad (28)$$

where *qf* refers to the heat flow rate that is evacuated from structure contacts at fixed cooled temperatures.

The expression can be written as a linear system then using mean square operator the appropriate vector $qf_d$ that matched the fixed temperature vector $Td_j$, can be easily approximated in few iterations.

The board thermal behaviour is analysed when a fixed temperature of 70 °C is assumed on two distinct zones, on the rear surface of the board ($zd = 0$), that have a length of 6 mm (*Ld*), and a width of 127 mm (*Wd*).

The *yc* center is located at half board width and their respective *xc* center position are 3 mm and 97 mm.

A wedge imperfect contact is simulated considering a thermal resistance of 2.5 °C/cm$^2$W.

The temperatures predictions are reported in tab. 9 but the model accuracy is based this time on the relative error calculation, as a result of dual boundary conditions.

**Table 9. Component junction and case temperatures for mixed cooling**

| | | | | | | M. Model | | N. Model | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Gravity axis | Device | *Lc* | *Wc* | *Hc* | *Pc* | $T_{J\text{-}M}$ | $T_{C\text{-}M}$ | $T_{J\text{-}N}$ | $T_{C\text{-}N}$ | $(T_M\text{-}T_N)/(T_N)$ | |
| | | [mm] | [mm] | [mm] | [W] | [°C] | [°C] | [°C] | [°C] | [%] | [%] |
| –z | MLF64 | 9 | 9 | 0.9 | 0.75 | 98.4 | 96.3 | 97.9 | 95.6 | 0.5 | –0.1 |
| | MLF32 | 5 | 5 | 0.9 | 0.5 | 105.0 | 101.7 | 103.2 | 99.8 | 1.8 | –5.4 |

* $T_A = 85$ °C and $Td_{1,2} = 70$ °C

The estimation of the heat flow rate, which is leaving the PWB from both cooled wedges, is 5.48 W.

This value agrees with the prediction of 5.4 W provided by the numerical model and demonstrates that the board upper and lower surfaces are receiving external heat fluxes from ambient.

### Multi-layered chip location

The spotlighted approach describes a simplified analytical model which is resumed to a two layered board but a more detailed stack-up can be done. A new set of interlayer boundary condition relationship has to be defined.

Eventually, the z-axis thermal profile formulae must be corrected depending on the selected board layers number, for instance $\omega r_{m,n,i}(z)$ and $\omega u_{m,n,i}(z)$ are rewritten as:

$$\omega r_{m,n,j}(z) = \frac{\dfrac{\chi l_j}{kz_j}\gamma(r_{m,n,j}, z) + ch(r_{m,n,j} z)}{(hr - \chi l_1)\prod_{i=1}^{j-1}(\beta_i \chi l_{i+1} + \alpha)} \quad \text{for} \quad j \neq 1 \tag{29a}$$

$$\chi l_i = \frac{\lambda_i \chi l_{i+1} + \delta_i}{\beta_i \chi l_{i+1} + \alpha_i} \tag{29b}$$

$$\omega u_{m,n,j}(z) = \frac{\prod_{i=Nl-1}^{j}(\beta_i \chi u_{i+1} + \alpha)\left[\dfrac{\chi u_j}{kz_j}\gamma(r_{m,n,j}, z) + ch(r_{m,n,j} z)\right]}{(\chi u_{Nl} + ht)ch(r_{m,n,Nl} Hb) + \left[kz_{Nl}(r_{m,n,Nl})^2 + \dfrac{\chi u_{Nl}}{kz_{Nl}} ht\right]\gamma(r_{m,n,Nl}, Hb)} \quad \text{for } j \tag{30a}$$

with

$$\chi u_{i+1} = \frac{\delta_i - \alpha_i \chi u_i}{\beta_i \chi u_i - \lambda_i} \tag{30b}$$

The performance comparison is not displayed in this paper but turns out to be fulfilling.

### Conclusions

A pragmatic approach has been established with the aim of supplying a practical solution to early identify the potential issues of board cooling and so to achieve a more efficient design. The proposed analytical modelling is based, at first, on the assumptions that the board shape is a parallelepiped, its multilayered structure is summed up by two linear orthotropic layers in perfect thermal contact and its buried chips are assimilated to collapsed sources. However, the number of orthotropic layers can be increased in order to analyse disparate embedded chip stack up. As significant benefits, the model definition allows to take into account a set of distinct heat transfer coefficients as well as simulate thermal impact of electronic components by the means of CTM.

This method appears to be rational and able to produce acceptable predictions for mixed free convection and conduction cooling mode.

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## Appendix

### z-axis thermal profile of source located on board lower and upper surfaces

$$\omega r_{m,n,1}(z) = \frac{1}{hr - \chi l_1}\left[\frac{\chi l_1}{kz_1}\gamma(r_{m,n,1}, z) + ch(r_{m,n,1} z)\right] \tag{A1}$$

$$\omega r_{m,n,2}(z) = \frac{1}{(\beta_1 \chi l_2 + \alpha_1)(hr - \chi l_1)}\left[\frac{\chi l_2}{kz_2}\gamma(r_{m,n,2}, z) + ch(r_{m,n,2} z)\right] \tag{A2}$$

$$\omega u_{m,n,1}(z) = \frac{(\beta_1 \chi u_2 + \alpha_1)\left[\frac{\chi u_1}{kz_1}\gamma(r_{m,n,1}, z) + ch(r_{m,n,1} z)\right]}{(\chi u_2 + ht)ch(r_{m,n,2} Hb) + \left[kz_2 (r_{m,n,2})^2 + \frac{\chi u_2}{kz_2} ht\right]\gamma(r_{m,n,2}, Hb)} \tag{A3}$$

$$\omega u_{m,n,2}(z) = \frac{\dfrac{\chi u_2}{kz_2}\gamma(r_{m,n,2}, z) + ch(r_{m,n,2} z)}{(\chi u_2 + ht)ch(r_{m,n,2} Hb) + \left[ kz_2 (r_{m,n,2})^2 + \dfrac{\chi u_2}{kz_2} ht \right] \gamma(r_{m,n,2}, Hb)} \tag{A4}$$

$$\alpha_i = ch(r_{m,n,i+1} z_i)ch(r_{m,n,i} z_i) - \frac{kz_{i+1}}{kz_i} r_{m,n,i+1}\gamma(r_{m,n,i} z_i)sh(r_{m,n,i+1} z_i)$$

$$\delta_i = kz_{i+1} r_{m,n,i+1} sh(r_{m,n,i+1} z_i)ch(r_{m,n,i} z_i) - kz_i r_{m,n,i} ch(r_{m,n,i+1} z_i)sh(r_{m,n,i} z_i) \tag{A5}$$

$$\beta_i = \frac{1}{kz_{i+1}}\gamma(r_{m,n,i+1} z_i)ch(r_{m,n,i} z_i) - \frac{1}{kz_i}\gamma(r_{m,n,i} z_i)ch(r_{m,n,i+1} z_i)$$

$$\lambda_i = ch(r_{m,n,i+1} z_i)ch(r_{m,n,i} z_i) - \frac{kz_i}{kz_{i+1}}(r_{m,n,i+1})^2\gamma(r_{m,n,i} z_i)sh(r_{m,n,i+1} z_i)$$

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