THERMAL MANAGEMENT OF THE HOTSPOTS IN 3-D INTEGRATED CIRCUITS

by

Kang-Jia WANG[a*], Hong-Chang SUN[b,c*], Cui-Ling LI[d], Guo-Dong WANG[a], and Hong-Wei ZHU[a]

[a] School of Physics and Electronic Information Engineering, Henan Polytechnic University, Jiaozuo, China
[b] School of Control Science and Engineering, Shandong University, Jinan, China
[c] Shandong Dawei International Architectural Design Co., LTD, Mechanical and Electrical Design Institute, Jinan, China
[d] College of Information Engineering, Huizhou Economics and Polytechnic College, Huizhou, China

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Vertical integration for microelectronics possesses significant challenges due to its fast dissipation of heat generated in multiple device planes. This paper focuses on thermal management of a 3-D integrated circuit, and micro-channel cooling is adopted to deal with the 3-D integrated circuitthermal problems. In addition, thermal through-silicon vias are also used to improve the capacity of heat transmission. It is found that combination of microchannel cooling and thermal through-silicon vias can remarkably alleviate the hotspots. The results presented in this paper are expected to aid in the development of thermal design guidelines for 3-D integrated circuits.

Key words: *thermal*, 3-D *integrated circuit, micro-channel, thermal through-silicon vias*

Introduction

In recent years, the 3-D integrated circuit (3D-IC), integrating multiple device layers in the vertical direction, offers several advantages over its traditional 2-D partner in reducing its average wire length, wire delay, power consumption, footprint and others [1-3]. The 3D--IC technology is an emerging technology for the near future and has received a lot of attention in the semiconductor community. However, as the package density increases, the heat quantity in each unit volume becomes high, which will greatly increase the working temperature of the device. The problems of heat dissipation are more serious and have caught much more attention than those in the traditional single IC package. Hence, thermal management for 3D-IC is becoming a major concern [4-10].

The micro-channel cooling technology, emerging as a powerful tool to remove the excessive heat in the 3-D chips, has received considerable attention [11-19]. Micro-channels are embedded in the interlayer regions of the 3D-IC, where the coolant is pumped through the micro-channels and removes the heat inside 3D-IC by thermal conduction and convection. It has been demonstrated that the micro-channel cooling can help remove the waste heat of

* Corresponding author's, e-mail: konka05@163.com; kk121618@163.com

200-400 W/cm^2 and has the potential to reach as high as 1000 W/cm^2 [20, 21]. In addition, the dummy thermal through-silicon vias (TTSV) that have no electrical significance are also used to alleviate the 3D-IC thermal problems because they can help in reducing the chip temperature by increasing the thermal conductance between different active dies. The heat usually transfers preferentially through the TTSV due to the high heat conductivity. In this paper, we mainly solve the hotspot problems in the 3D-IC by combining the micro-channel cooling with the TTSV. The results show that the method of combining the micro-channel cooling with the TTSV can alleviate the hotspots by decreasing the temperature effectively. The method can be effectively used as design guidelines in 3D-IC thermal management studies.

The 3D-IC thermal models

Figure 1 shows the 3D-IC structure, where the different dies are bonded with the face-to-back form through the bonding layer. Generally, a heat spreader and/or heat sink are assumed to be attached to the bottom-most die. The effect of the heat spreader/sink can be modeled as a convective heat transfer coefficient on the bottom surface of the bottom-most die. The top surface of the die stack, which is typically attached to the electronic package, is assumed to be adiabatic, since the thermal resistance of the electronic package is typically much larger than that of the heat spreader/sink. All the other side surfaces are assumed to be adiabatic.

The derivation of the conventional compact model for heat conduction in solids begins with the governing equation of heat transfer in solids, which can be written in the differential form as [22]:

$$C_{\mathrm{v}} \frac{\mathrm{d}T}{\mathrm{d}t} + (-k\nabla^2 T) = \dot{q} \tag{1}$$

where C_{v} is the volumetric specific heat of the material, T – the temperature of the control volume, k – the thermal conductivity of the material, and $\dot{q}$ – the volumetric rate of generation of the heat inside the volume.

Figure 2 shows the 3D-IC structure with integrated micro-channel cooling, where the micro-channels are embedded in the bulk regions of the 3D-IC. The coolant is pumped through the micro-channels and removes the heat inside 3D-IC by thermal conduction and thermal convection.

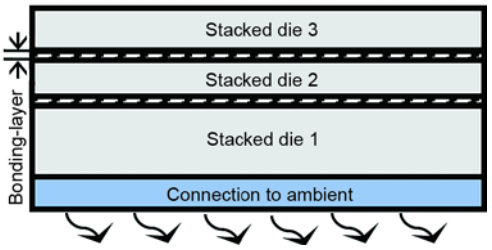

Figure 1. The 3D-IC structure

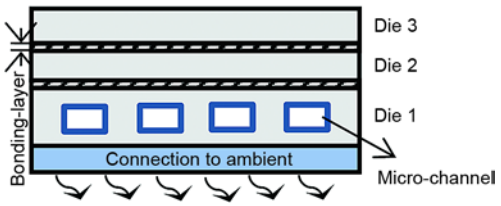

Figure 2. The 3D-IC structure with integrated microchannel cooling

In the micro-channel cooled 3D-IC, the energy conservation equation for heat transfer in a control volume of the liquid can be written [22]:

$$C_{\mathrm{v}}\frac{\mathrm{d}T}{\mathrm{d}t}+(-k\nabla^2 T)+C_{\mathrm{v}}\vec{\mathrm{u}}\nabla T=\dot{q} \tag{2}$$

when compared to eq. (1), eq. (2) contains an added term on the left hand side, where $\vec{\mathrm{u}}$ is the velocity of outflow of the fluid at the surface of the control volume. This term indeed represents the net outflow of heat from the control volume due to convection.

Figure 3 shows the 3D-IC with the integrated micro-channel cooling and TTSV. These TTSV, which have no electrical significance, help in reducing the chip temperature by increasing the thermal conductance between different active dies. The TTSV can increase the interlayer thermal conductivity, as a result, a more uniform thermal profile can be obtaine.

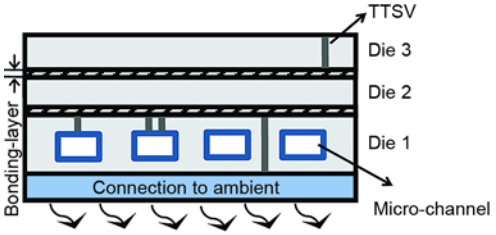

Figure 3. The 3D-IC structure with integrated microchannel cooling and TTSV

When the TTSV are introduced, the thermal conductivity of the die can be described as effective thermal conductivity k_{eff}, which is written:

$$k_{\mathrm{eff}}=k_{\mathrm{mat}}\left(1-\frac{A_{\mathrm{TTSV}}}{A_{\mathrm{die}}}\right)+k_{\mathrm{TTSV}}\frac{A_{\mathrm{TTSV}}}{A_{\mathrm{die}}} \tag{3}$$

where k_{mat} and k_{TTSV} are the thermal conductivity coefficients of the active die and the TTSV, respectively, A_{die} is the area of die, and A_{TTSV} is the area of the TTSV.

Model verification

The 3D-IC thermal model that we use to study in this paper has two dies. As shown in tab. 1, die-1 and die-2, which have the same thermal conductivity coefficient of 120 W/mK, are assumed to have the volume of 10 mm by 10 mm by 5 mm and 10 mm by 10 mm by 2 mm, respectively. The bonding-layer with thermal conductivity coefficient of 20 W/mK has the volume of 10 mm by 10 mm by 0.5 mm. As shown in fig. 4, from the top view of each die, the heat sources with volume of 1 mm by 1 mm by 1 mm (co-ordinate position: 4.5 mm < < x < 5.5 mm, 2.0 mm < y < 3.0 mm, 4.0 mm < z < 5.0 mm, heat generation: $6.0 \cdot 10^9$ W/m^3) and volume of 1 mm by 1 mm by 1 mm (co-ordinate position: 4.5 mm < x < 5.5 mm, 7.0 mm < y < 8.0 mm, 6.5 mm < z < < 7.5 mm, heat generation: $2.0 \cdot 10^9$ W/m^3) are placed in die-1 and die-2, respectively. In the

Table 1. The relevant parameters of the model

Parameter	Value	Unit
Material properties		
Die-1	120	$Wm^{-1}K^{-1}$
Bonding-layer	20	$Wm^{-1}K^{-1}$
TTSV	600	$Wm^{-1}K^{-1}$
Die-2	120	$Wm^{-1}K^{-1}$
Size		
Die-1	10 × 10 × 5	m^3
Die-2	10 × 10 × 2	m^3
Bonding-layer	10 × 10 × 0.5	m^3
Cooling liquid settings		
Mass-flow	20	mgs^{-1}
Inlet fluid temperature	10	°C
Heat capacity	4182	$Jkg^{-1}K^{-1}$
Thermal conductivity	0.6	$Wm^{-1}K^{-1}$
Boundary conditions		
Temperature ambient	25	°C
Co-efficient (bottom)	1000	$Wm^{-1}K^{-1}$

micro-channel cooling, water is used as cooling liquid, the mass flow is 20 mg/s, inlet fluid temperature is 10 °C, the heat capacity is 4182 J/kg°C and the thermal conductivity is 0.6 W/mK. At the bottom of the bottom-most die, the convective heat transfer coefficient is set to be 1000 W/m^{2}K, and the other side surfaces are assumed to be adiabatic.

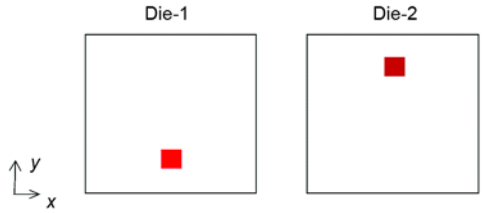

Figure 4. Heat generation distribution in each die of the two-die 3D-IC

In the following content, there are three different cases to study. They are the 3D-IC without micro-channel and TTSV, the 3D-IC with micro-channel, and the 3D-IC with micro-channel and TTSV.

Figure 5 shows temperature curve along the *y*-direction at x = 5.0 mm, z = 5.0 mm without micro-channel and TTSV, where the temperature reaches the highest at the heat source position.

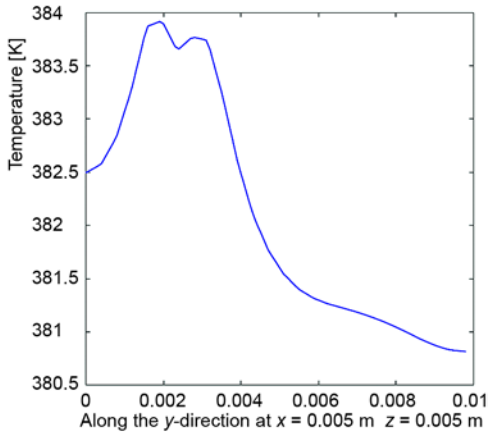

Figure 5. Temperature curve along the y-direction at x = 5.0 mm, z = 5.0 mm

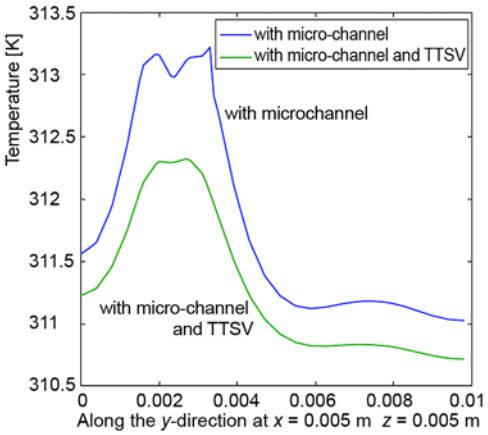

Figure 6. Temperature curve along the y-direction at x = 5.0 mm, z = 5.0 mm

The micro-channel with height of 1.0 mm and width of 2.0 mm is embedded in die-1. The micro-channel is along the x-direction, and it is under the heat source of the die-1, where TTSV (co-ordinate position: 4.5 mm < x < 5.5 mm, 2.0 mm < y < 3.0 mm, 3.0 mm < z < 4.0 mm) is designed between the heat source and the micro-channel. So the heat can flow preferentially into the micro-channel through the TTSV due to its high thermal conductivity.

Figure 6 shows the temperature curves along the y-direction at x = 5.0 mm, z = 5.0 mm, where the blue curve represents the temperature curve of 3D-IC with micro-channel cooling and the green curve represents the temperature curve of 3D-IC with micro-channel and TTSV. Comparing fig. 6 with fig. 5, we find that the micro-channel cooling can decrease the temperature by 70 K. In addition, we also find the temperature declines more effectively in the hotspot position than other places due to the impact of TTSV as shown in the fig. 6.

Conclusion

In this paper, the method of combining micro-channel cooling with the thermal through-silicon vias to alleviate the hotspots is studied. The results show that the method can offer help in dealing with the hotspots. The results presented in this paper are expected to aid in the development of thermal design guidelines for 3D-IC.

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