AN ANALYTICAL THERMAL MODEL FOR THREE-DIMENSIONAL INTEGRATED CIRCUITS WITH INTEGRATED MICRO-CHANNEL COOLING

by

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An analytical thermal model is developed for N-die stacked chips with integrated micro-channels cooling. The model is implemented with some mathematical software. Comparison of the temperature predicted by the proposed model with some computer fluid dynamics software numerical results show excellent agreement, and the maximal relative error is less than 4.0%.

Key words: *thermal, 3-D integrated circuit, micro-channel*

Introduction

With the development of modern technology, consumers demand more functions in their hand-held devices. The urgent need for more memory in a limited space is increasing, and integration of various functions into a same package is becoming extremely crucial. Over the past few years, die stacking has emerged as a powerful tool for satisfying these challenging integrated circuit (IC) packaging requirements [1-3].

Expanding a design space of an IC into a 3-D partner (3-D IC) reduces significantly its average wire length, delay, power consumption, and footprint. Although electrical benefits are proved to have great improvements in stacked IC packages, stacking of multiple circuit layers makes effective cooling more challenging [4, 5]. The problems of heat dissipation have become more serious than those in the traditional single IC package, and therefore much attention has been caught. Hence, the thermal management for 3-D IC is becoming major concerns [6-8].

There are a lot of achievements about the thermal analysis of the 3-D IC. In [9], a quadratic uniformity modeling approach was proposed to get the expression of the temperature distribution of the 3-D IC chip and the thermal dissipation of the laminated chip was optimized. In [10], the effective thermal conductivity of the 3-D IC was proposed. In [11], the theory of fluid dynamics was used to study the temperature distribution of multi-pass hole stack chip. In [12], the 1-D analytical thermal model for N-die stacked chips was suggested. In [13], an analytical thermal model for 3-D IC considering through silicon was established. In this paper, we propose an analytical thermal model for 3-D IC with integrated micro-channels cool-

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ing. The model is analyzed and validated numerically by a mathematical software. Compared with numerical solutions, our results show an accurate and rapid prediction of temperature distribution of each die. In addition, the model is simple and easy for calculation.

The analytical thermal model

As shown in fig. 1(a), the 3-D IC structure consists of N-silicon active layers that are bonded in the form of face-to-back. Micro-channels are integrated in the bulk at bottom of each device-layer. The devices on each plane are considered as isotropic heat sources and each device is modeled as a thin layer on the top surface of the bulk layer. The lateral boundaries of the 3-D IC are considered to behave adiabatically, so the heat flow is 1-D. The R_{pk} is the thermal resistance of the package, $R_{j,\mathrm{up}}$ is the thermal resistance between the j^{th} device and the top wall of the micro-channel in the j^{th} bulk layer, it is associated with the micro-channel layer. The $R_{j,\mathrm{dot}}$ is the thermal resistance between the bottom wall of the micro-channel in the j^{th} bulk layer and the $(j-1)^{\mathrm{th}}$ device, which is associated with bonding layer and the micro-channel layer. The $R_{j,b}$, R_{j,c_up}, and R_{j,c_dot} represent the thermal resistance of the bonding layer, the micro-channel top wall and the micro-channel bottom wall, respectively, so $R_{j,\mathrm{up}}$ and $R_{j,\mathrm{dot}}$ can be written as $R_{j,\mathrm{up}} = R_{j,c\_\mathrm{up}}$ $(j < n)$ and $R_{j,\mathrm{dot}}=R_{j,b} + R_{j,c\_\mathrm{dot}}$ $(j > 1)$, respectively.

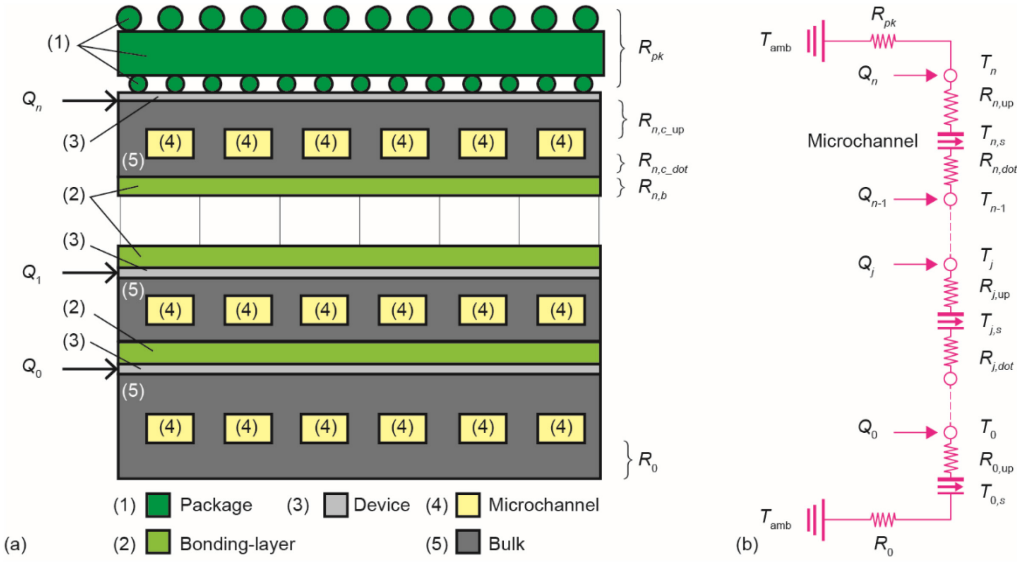

Figure 1. A general 3-D IC with micro-channels and its thermal model

Based on the previous assumptions, fig. 1(b) shows 1-D heat transfer model, where T_j represents the temperature of the j^{th} device, $T_{j,s}$ – the wall temperature of the micro-channel that integrated in the j^{th} bulk layer, Q_j – the heat generated from the j^{th} device, and T_{amb} the ambient temperature. Heat is generated in the resistance network at each node and flows to the ambient through either the micro-channels or the package. In the steady-state case, the temperature in each die is governed by equations of energy conservation:

– for $j = n$, we have:

$$\frac{T_n - T_{\mathrm{amb}}}{R_{\mathrm{pk}}} + \frac{T_n - T_{n,s}}{R_{n,\mathrm{up}}} = Q_n, \qquad (j = n) \tag{1}$$

– for $j = 1, 2,\ldots, n-1$, we have:

$$\frac{T_j - T_{j+1,s}}{R_{j+1,\mathrm{dot}}} + \frac{T_j - T_{j,s}}{R_{j,\mathrm{up}}} = Q_j, \qquad (j = 0, 1, ..., n-1) \tag{2}$$

Micro-channel thermal analysis

It is supposed that the micro-channels are made in a monolithic layer that is inserted between existing dies and in perfect thermal contact with them. The geometry is presented in fig. 2.

It is assumed that the flow in the micro-channel is laminar and the velocity profile is fully developed once it reaches the heated zone. According to Newton cooling equation, we have:

$$\Phi = h_f A \Delta T \tag{3}$$

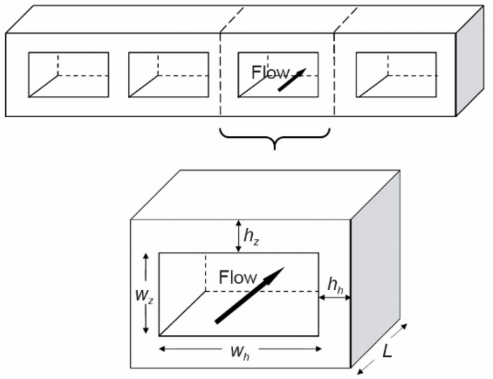

Figure 2. The structure of the micro-channel

where h_f is the convection heat transfer coefficient, and A – the area of interface where convection takes places. Convective heat transfer between solid and fluid can be characterized by the convective thermal resistance:

$$R_{\mathrm{conv}} = \frac{1}{h_f A} \tag{4}$$

where the convection heat transfer coefficient, h_f, that we can get from eq. (5):

$$h_f = \frac{\mathrm{Nu}\ k_f}{D_{\mathrm{h}}} \tag{5}$$

where Nu is the Nusselt number, k_f – the coolant's thermal conductivity, and D_{h} – the hydraulic diameter and is given by eq. (6) for rectangular channels:

$$D_{\mathrm{h}} = \frac{4A_{\mathrm{ch}}}{P_{\mathrm{ch}}} \tag{6}$$

where A_{ch} and P_{ch} denote the channel cross-sectional area and channel perimeter, respectively. Combining eq. (4) with eq. (5), we can get:

$$R_{\mathrm{conv}} = \frac{D_{\mathrm{h}}}{\mathrm{Nu}\ k_f A} \tag{7}$$

Temperature is supposed to be kept uniform over the micro-channel wall surface. The Nusselt number is estimated by a polynomial as shown in eq. (8) [14]:

$$\mathrm{Nu} = 0.0275\left(\frac{w_z}{w_h}\right)^2 + 0.631\frac{w_z}{w_h} + 2.32 \tag{8}$$

Combining eq. (6) with eq. (7), we can get:

$$R_{\mathrm{conv}} = \frac{w_h w_z}{\mathrm{Nu}\, k_f (w_h + w_z)^2 l} \tag{9}$$

Supposing that the inlet fluid temperature of the j^{th} micro-channel is $T_{j,\text{in}}$, outlet fluid temperature of the j^{th} micro-channel is $T_{j,e}$, the $T_{j,\text{in}}$, $T_{j,s}$, and $T_{j,e}$ have the relation [14]:

$$\ln\frac{T_{j,s}-T_{j,e}}{T_{j,s}-T_{j,\text{in}}}=-\frac{1}{R_{\text{conv}}\dot{m}c_p} \tag{10}$$

where $\dot{m}$ is the mass flow, and c_p – the heat capacity. For the j^{th} micro-channel, we have:

$$\begin{aligned}&\frac{T_j-T_{j,s}}{R_{j,\text{up}}}+\frac{T_{j-1}-T_{j,s}}{R_{j,\text{dot}}}=\dot{m}c_p(T_{j,e}-T_{j,\text{in}})\quad (j=1,2,3,...,n)\\&\frac{T_0-T_{0,s}}{R_{0,\text{up}}}+\frac{T_{\text{amb}}-T_{0,s}}{R_0}=\dot{m}c_p(T_{0,e}-T_{0,\text{in}})\quad (j=0)\end{aligned} \tag{11}$$

Equations (1), (2), (10), and (11) represent $3(n+1)$ equations that can be easily solved to determine the $3(n+1)$ variables T_0, T_1,…, T_n; $T_{0,s}$ $T_{1,\text{s}}$,…, $T_{n,s}$; $T_{0,e}$, $T_{1,e}$,…, $T_{n,\text{e}}$. By careful rearrangement of equations, eqs. (1), (2), (10), and (11) can be written:

$$[\text{A}]\text{T}=\text{B} \tag{12}$$

Figure 3. Structure of matrix [A]
(*for color image see journal web site*)

where [A] is a $3(n+1)\times3(n+1)$ sparse matrix, which $(n+1)$ denotes the total number of the stacked chips. The element structure of matrix [A] is shown in the fig. 3, where the * sign represents the non-zero element, among them, the colorized elements appear with great regularity. The T is a column array of temperature with the element structure as shown in the fig. 4. The B is a known column, which can be obtained by the initial conditions and the relevant parameters of the model. This sparse matrix equation can be efficiently solved by existing sparse solver such as KLU to obtain the steady-state temperatures.

$$[T_n, T_{n\text{-}1}, T_{n\text{-}2},\ldots, T_0, T_{n,s}, T_{n\text{-}1s}, T_{n\text{-}2,s},\ldots, T_{0,s}, T_{n,e}, T_{n\text{-}1,e}, T_{n\text{-}2e},\ldots, T_{0,e}]$$

Figure 4. Structure of column B

Model verification

In this section, the models of two-die 3-D IC and three-die 3-D IC that integrated with micro-channels are verified, respectively. Since the overall model is a symmetric structure (as shown in fig. 1). Here just part structure is analyzed (as shown in fig. 5).

To minimize the model complexity, assuming that the device, bonding layer, and bulk of different dies have the same structure, the ambient temperature is set to be 25 °C. Water is used as cooling liquid, the mass flow is 20 mg/s, inlet fluid temperature is 10 °C, the heat capacity and thermal conductivity are 4182 J/(kg°C) and 0.6 W/(m°C), respectively.

The channel length, l, height, w_z, and width, w_h, are 10, 50, and 150 μm, respectively, wall width, h_h, and height, h_z, are both 15 μm, the thermal resistance, $R_{j,\mathrm{up}}$, $R_{j,\mathrm{dot}}$, R_{pk}, and R_0 are 2, 10, 20, and 4 °C/W, respectively.

Two-die stacked model validation and analysis

In this section, we analyze two different heat power cases of a two-die 3-D IC, that is, the heat flow Q_1 and Q_0 are assigned $2W$-$1W$ and $1W$-$1W$ in case 1 and case 2, respectively. The results comparison between CFD software and our proposed model is shown in tab. 1, where the deviation is in the range of 1.2-3.0%.

Three-die stacked model validation and analysis

We analyze three different cases of a three-die 3-D IC. The heat flow Q_2, Q_1, and Q_0 are assigned $3W$-$1W$-$1W$, $1W$-$3W$--$1W$, and $1W$-$1W$-$1W$ in the case 1, case 2, and case 3, respectively. The comparison between CFD software and our proposed model is shown in the tab. 2. According to the tab. 2, it finds that the relative deviation between the results is below 4.0% in different cases.

From all previous validation and analysis, we find that the comparison of the temperature predicted by the proposed model with CFD simulations shows excellent agreement. Moreover, the analytical model is simple and easily to solve. In the light of this work, it seems that the analytical model provides valuable data and insight in temperature management of the 3-D IC with micro-channels cooling.

Conclusion

This paper presents an analytical thermal model of 3-D IC with integrated micro-channel cooling. The model is validated through a two-die 3-D IC, and a three-die 3-D IC using a mathematical software,

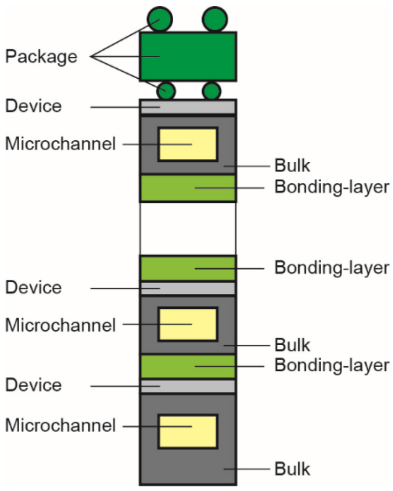

Figure 5. Part structure of the model

Table 1. Comparisons between CFD software and our proposed method

	Method	T1	T0
Case 1	CFD	34.98 °C	29.12 °C
	Ours	35.41 °C	29.97 °C
	Deviation	1.22%	2.92%
Case 2	CFD	29.21 °C	27.83 °C
	Ours	28.53 °C	27.44 °C
	Deviation	2.33%	1.40%

Table 2. Comparisons between CFD software and our proposed method

	Method	T2	T1	T0
Case 1	CFD	44.07 °C	35.26 °C	29.56 °C
	Ours	44.15 °C	34.54 °C	30.31 °C
	Deviation	0.18%	2.08%	2.47%
Case 2	CFD	35.52 °C	42.72 °C	31.39 °C
	Ours	35.15 °C	41.87 °C	32.66 °C
	Deviation	1.05%	2.03%	3.89%
Case 3	CFD	29.17 °C	28.91 °C	27.52 °C
	Ours	29.99 °C	29.85 °C	27.91 °C
	Deviation	2.73%	3.15%	1.40%

respectively. Compared with the CFD numerical solutions, our results show excellent agreement, for which the relative deviation is less than 4.0%. Moreover, the proposed model is simple.

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