ANALYTICAL MODELING OF MULTI-LAYERED PRINTED CIRCUIT BOARD USING MULTI-STACKED VIA CLUSTERS AS COMPONENT HEAT SPREADER

by

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In order to help the electronic designer to early determine the limits of the power dissipation of electronic component, an analytical model was established to allow a fast insight of relevant design parameters of a multi-layered electronic board constitution. The proposed steady-state approach based on Fourier series method promotes a practical solution to quickly investigate the potential gain of multi-layered thermal via clusters. Generally, it has been shown a good agreement between the results obtained by the proposed analytical model and those given by electronics cooling software widely used in industry. Some results highlight the fact that the conventional practices for Printed Circuit Board modeling can be dramatically underestimate source temperatures, in particular with smaller sources. Moreover, the analytic solution could be applied to optimize the heat spreading in the board structure with a local modification of the effective thermal conductivity layers.

Key words: *analytical printed circuit board modeling, effective thermal conductivity, copper via impact*

Introduction

Electronic components are continuously getting closer to the chip size and require more and more an efficient thermal management to limit the temperature excess to preserve component reliability. For still air conditions, the heat spreading of these miniaturized devices is henceforth done through the surrounding metallic planes of its multilayer printed circuit board (PCB). Moreover, initially designed to realize the electrical interconnection through dielectric layer between the various embedded metallic layers, via concept is today used to make chip pad attachment to the high thermal conductive planes of the board. Thus a set of metal planes are connected together from via matrix with the aim to locally create an efficient thermal path to drain the heat in the heart of board structure. The PCB has to be considered as the dominant remover of component heat and an accurate 3-D prediction of temperature distribution is mandatory for evaluating the temperatures of its sensitive Surfaces Mounted Devices.

More than ever, electronic board designers are aware to deliver an optimized board design to eliminate potential reliability issues of high powered devices due to excessive temperature beyond manufacturer limit. The ability to know the sensitivity of component temperatures to the

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relevant board design parameters, such as the use of thermal vias, is today a crucial stake. Last generation of miniaturized electronic component is reinforcing the need for simulating in thinner details its vicinity board architectures with a minimum of set-up, pertinent assumptions and low computation time is henceforth mandatory. Thus the conventional assumptions for electronic board thermal modeling are discussed with the aim to check the pertinence of existing methods and to quantify their inherent uncertainty. For instance, the PCB effective thermal conductivity is a major parameter for electronic thermal analysis so its conventional calculation technique was debated.

The present study is based on the use of an analytical thermal model for better discerning the sensitive parameters and managing solution accuracy. The objective of this work is to promote a systematic characterization of the design of electronic boards, at an early stage. Analytical methods are easy to use, effortless to implement, as well as to have no complex meshing or convergence rules to master [1]. So the proposed approach highlights a case in cooling arsenal techniques for spreading heat away from overheated sources.

Analytical model and assumptions

The proposed analytical formulation allows fast evaluation of temperature profile of constitutive dielectric or conductive layers of an electronic board under steady state conditions. The cuboids board shape, pictured in fig. 1, is considered cooled by coupled convection and radiation heat exchanges to enable potential infrared measurement validation at laboratory boundary conditions. Like in many conventional studies on PCB thermal behavior, the four lateral edges are assumed to be adiabatic due to their very low thickness. Therefore top and rear surfaces are exposed to a specific uniform heat transfer coefficient according to the Newton's law, named respectively *ht* and *hr*. Both coefficients combine convection and radiation effects and allow us to take into account the gravity orientation.

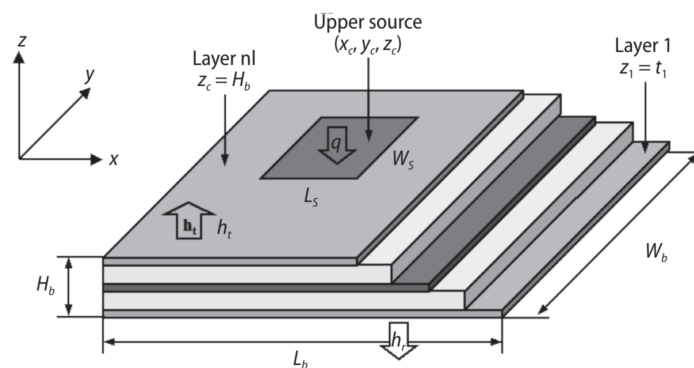

Figure 1. Definition of geometric parameters of the analytical model

Thus the heat of the planar source is only transfer through these external surfaces to the ambient, defined as T_A. The planar source can be located on upper or lower board external surfaces. Its heat flow rate q is assumed uniform over the source. The board shape is always approximated by a rectangular or a square geometry. Its overall length, width and thickness are, respectively, defined by *Lb*, *Wb*, and *Hb*. Each interface of adjacent layer is considered in perfect thermal contact.

The set of equations describing the proposed conduction model and its boundary conditions are summarized below. The subscript letter *i* is the index to the *nl* constitutive layers of the electronic board and x, y, and z are Cartesian co-ordinates.

If $\theta_i(x,y,z) = T_i(x,y,z) - T_\infty$ is the difference between the local and the reference temperatures, the generalized steady-state governing equation depends on a set of axial thermal conductivity values, defined by *kx*, *ky* or *kz*:

$$kx_i \frac{\partial^2 \theta_i(x,y,z)}{\partial x^2} + ky_i \frac{\partial^2 \theta_i(x,y,z)}{\partial y^2} + kz_i \frac{\partial^2 \theta_i(x,y,z)}{\partial z^2} = 0 \quad \text{for} \quad i = 1, nl \tag{1}$$

Edge boundary conditions:

$$kx_i \frac{\delta \theta_i(x,y,z)}{\delta x}\bigg|_{x=0,Lb} = 0 \quad \text{and} \quad ky_i \frac{\delta \theta_i(x,y,z)}{\delta y}\bigg|_{y=0,Wb} = 0 \quad \text{for} \quad i = 1, nl \tag{2}$$

Board's boundary conditions, when the heating source is located on top surface ($i = nl$):

$$-kz_{nl} \frac{\delta \theta_{nl}(x,y,z)}{\delta z}\bigg|_{z=Hb} = ht\theta_{nl}(x,y,Hb) - u(x,y) \quad \text{and} \quad -kz_1 \frac{\delta \theta_1(x,y,z)}{\delta z}\bigg|_{z=0} = -hr\theta_1(x,y,0) \tag{3}$$

Board's boundary conditions, for a heating source located on bottom surface ($i = 1$):

$$-kz_1 \frac{\delta \theta_1(x,y,z)}{\delta z}\bigg|_{z=0} = -hr\theta_1(x,y,0) + l(x,y) \quad \text{and} \quad -kz_{nl} \frac{\delta \theta_{nl}(x,y,z)}{\delta z}\bigg|_{z=Hb} = ht\theta_{nl}(x,y,Hb) \tag{4}$$

where $u(x,y)$ and $l(x,y)$ are the prescribed heat flux function of the upper and lower board surfaces.

Interlayer temperature continuity and flux conversion boundary conditions:

$$\theta_{i+1}(x,y,z)\big|_{z=z_i} = \theta_i(x,y,z)\big|_{z=z_i} \quad \text{for} \quad i = 1, nl-1 \tag{5}$$

$$kz_{i+1} \frac{\delta \theta_{i+1}(x,y,z)}{\delta z}\bigg|_{z=z_i} - kz_i \frac{\delta \theta_i(x,y,z)}{\delta z}\bigg|_{z=z_i} = 0 \quad \text{for} \quad i = 1, nl-1 \tag{6}$$

The 3-D temperature distribution of an upper or lower source location on a PCB has been solved using conventional Fourier series. The final practical solution of the temperature distribution can be written:

$$\theta_{m,n,i}(x,y,z) = \frac{qs}{LsWs} \sum_{m=0}^{M} \sum_{n=0}^{N} A_m B_n \cos\left(\frac{m\pi}{Lb}x\right) \cos\left(\frac{n\pi}{Wb}y\right) \omega_{m,n,i}(z) \tag{7}$$

The upper limit M and N of truncated Fourier series depend on accuracy requirements and m or n, are non-negative integers. Both relationships of the Fourier coefficient A_m and B_n are respectively:

$$A_m = 4As_m + \frac{Ls}{Lb}\delta_m \quad \text{where} \quad As_m = \frac{\sin\left(\frac{m\pi}{Lb}\frac{Ls}{2}\right)\cos\left(\frac{m\pi}{Lb}xc\right)}{m\pi + \delta_m} \tag{8}$$

$$B_n = 4Bs_n + \frac{Ws}{Wb}\delta_n \quad \text{where} \quad Bs_n = \frac{\sin\left(\frac{n\pi}{Wb}\frac{Ws}{2}\right)\cos\left(\frac{n\pi}{Wb}yc\right)}{n\pi + \delta_n} \tag{9}$$

where the source length, width and its center location are defined as Ls, Ws, xc, and yc. The Kronecker function δ is brought in the formulae to extend the domain validity to the indeterminate cases when m and/or n are equal to zero using the limit expressions of the equations As_m and Bs_n.

The z-axis thermal profile, $\omega(z)_{m,n,i}$, over the cross-section depends on the number of layers which are to be scrutinized to properly characterize the thermal behavior of the board. Its definition according to the boundary conditions of the upper or lower heating planar source such as if:

– the heating source is located on the upper board surface $\Rightarrow \omega(z)_{m,n,i} = \omega u(z)_{m,n,i}$, and
– the heating source is located on the lower board surface $\Rightarrow \omega(z)_{m,n,i} = \omega r(z)_{m,n,i}$.

$$\omega u_{m,n,i}(z) = \frac{Nu_{m,n,i}}{Du_{m,n,i}}\left[\omega c_{m,n,i}(z - z_{i-1}) + \frac{\chi u_{m,n,i}}{kz_i}\omega s_{m,n,i}(z - z_{i-1})\right]\mathrm{e}^{(z-Hb)\cdot r_{m,n,i}} \tag{10}$$

$$\omega r_{m,n,i}(z) = \frac{Nr_{m,n,i}}{Dr_{m,n,i}}\left[\omega c_{m,n,i}(z_i - z) + \frac{\chi r_{m,n,i}}{kz_i}\omega s_{m,n,i}(z_i - z)\right]\mathrm{e}^{-(z+Hb)\cdot r_{m,n,i}} \tag{11}$$

Formulas for $\chi u_{m,n,i}$ and $\chi r_{m,n,i}$ are:

$$\left|\begin{array}{ll} i = 1 & \Rightarrow \quad \chi u_{m,n,1} = hr \\ 1 < i < nl & \Rightarrow \quad \chi u_{m,n,i+1} = \dfrac{\alpha_{m,n,i} + \chi u_{m,n,i}\,\gamma_{m,n,i}}{\gamma_{m,n,i} + \chi u_{m,n,i}\,\beta_{m,n,i}} \end{array}\right. \tag{12}$$

$$\left|\begin{array}{ll} i = nl & \Rightarrow \quad \chi r_{m,n,nl} = ht \\ 1 \le i \le nl & \Rightarrow \quad \chi r_{m,n,i} = \dfrac{\alpha_{m,n,i+1} + \chi r_{m,n,i+1}\,\gamma_{m,n,i+1}}{\gamma_{m,n,i+1} + \chi r_{m,n,i+1}\,\beta_{m,n,i+1}} \end{array}\right. \tag{13}$$

while the others parameters of the solution are presented in the Appendix.

The exponential equation form was adopted to resolve large dimension ratio between heat source and PCB substrate, a constant issue for analytical thermal modeling approach.

The mean temperature of an arbitrary rectangular source of dimensions L_s and W_s, located at xc, yc, and zc co-ordinates, is obtained by integrating both cosine functions over the source region.

$$\overline{\theta_{m,n,i}}(x, y, z) = \frac{qs}{LsWs}\sum_{m=0}^{M}\sum_{n=0}^{N} A_m B_n \overline{A_m}\,\overline{B_n}\,\omega_{m,n,i}(z) \tag{14}$$

where the average Fourier coefficients are given by:

$$\overline{A_m} = 2\frac{Lb}{Ls}As_m + \delta_m \quad \text{and} \quad \overline{B_n} = 2\frac{Wb}{Ws}Bs_n + \delta_n \tag{15}$$

If several chips are mounted on the different PWB external surfaces, the solution for the temperature distribution may be obtained using the superposition principle.

$$\theta_{m,n,i}(x, y, z) = \sum_{j=1}^{ns}\frac{qs_j}{Ls_j Ws_j}\sum_{m=0}^{M_j}\sum_{n=0}^{N_j} A_{m,j} B_{n,j}\cos\left(\frac{m\pi}{Lb}x\right)\cos\left(\frac{n\pi}{Wb}y\right)\omega_{m,n,i}(z) \tag{16}$$

The Fourier coefficient $A_{m,j}$ and $B_{n,j}$ dedicated to each j heating source by:

$$A_{m,j} = 4\frac{\sin\left(\dfrac{m\pi}{Lb}\dfrac{Ls_j}{2}\right)\cos\left(\dfrac{m\pi}{Lb}xc_j\right)}{m\pi + \delta_m} + \frac{Ls_j}{Lb}\delta_m \tag{17}$$

$$B_{n,j} = 4\frac{\sin\left(\frac{n\pi}{Wb}\frac{Ws_j}{2}\right)\cos\left(\frac{n\pi}{Wb}yc_j\right)}{n\pi+\delta_n} + \frac{Ws_j}{Wb}\delta_n \tag{18}$$

Board physical geometries

The board analysis focuses on a high effective thermal conductivity test board with two external signal traces of 50 μm and two internal power-ground planes of 35 μm. This kind of multiple layers PCB is commonly named 2s2p board in regard of its 4 copper trace layers as shown in fig. 2. The PCB size for the presented study is fixed at 75 mm × 100 mm × 1.6 mm.

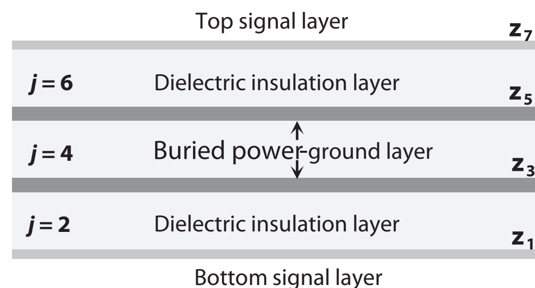

Figure 2. The 2s2p laminated cross-section overview

Therefore, 2s2p thermal test board is a stacked-up of 7 layers that alternates high and very low conductive layers. As a consequence, the effective thermal conductivity of this stack up is strongly anisotropic with a high heat spreading capability in-plane and a very poor one in cross-plane. Rightly underneath of top or bottom surface mounted devices, the dielectric thicknesses of the layers 2 and 6 usually lower than 250 μm have a major influence on the way the heat is removed. The present investigation deals with board parameters to assess the pertinence of analytical board modeling applied to small heating sources that are representative of copper pads of electronic component.

Effective thermal property calculations

Continuous copper trace signal layers of the electronics board

For a two-constituent printed wiring board material, the thermal property approximation is commonly based on parallel conduction model. Thus, the effective thermal conductivity *ke* is the weighted arithmetic mean of the thermal conductivities of the dielectric and copper materials.

$$ke = km + \phi(kf - km) \quad \text{where} \quad \phi = \frac{Sf}{Sm+Sf} \tag{19}$$

and *ke*, *km*, and *kf* are, respectively, the thermal conductivities of the derived equivalent material, the dielectric matrix, and the copper filler. *Sf* and *Sm*, represent the matrix and filler surfaces and ϕ the volume fraction of the filler.

Most of the time, in regard of conductivity ratio, the influence of matrix material is negligible and the effective conductivity is directly proportional to copper volume percentage [2]. For low copper covering area fraction, this conventional linear rule of mixture model returns a high thermal conductivity value that is clearly too optimistic for discontinuous and dispersed copper pads of a realistic signal layer of high density electronic board. The assumption of continuous heat conduction in parallel in both solids can be assumed as the upper bound model.

Discontinuous copper signal layers of the electronic board

It occurs that the electrical insulation due to the weak thermal conductivity of dielectric materials acts as a heat-spreading barrier [4]. This one has a major impact on the effective thermal conductivity of the derived compound material.

Many theoretical and empirical models have been defined to estimate the thermal conductivity of composite solid mixtures. In our case, the overall thermal conductivity of each layer depends in a complex arrangement on the geometry of the copper traces, disposed in an insulating material. Based on general effective medium theory, the relationship proposed by Bruggeman was considered to estimate the conductivity of dispersed heterogeneous shape particles:

$$ke = \frac{1}{4}\left(\gamma + \sqrt{\gamma^2 + 8kf\,km}\right) \quad \text{where} \quad \gamma = (3\phi - 1)kf + \left[3(1-\phi) - 1\right]km \tag{20}$$

This expression is defined as the lower bound model and is applicable to mixture when neither compound is continuous. By definition, PCB are complex multi-layered structures in which high thermal conductivity copper layers are sandwiched between low thermal conductivity glass-epoxy layers. Each i-layer has a specific j axial effective thermal conductivity $ke_{j,i}$.

Table 1 compiles, for 2s2p thermal test board under investigation, the values of the layer thickness, copper covering area factor and effective thermal conductivity derived of upper bound and lower bound models. The thermal conductivities of matrix and filler materials are assumed to be isotropic and respectively fixed at 0.3 W/mK for FR4 material and 400 W/mK for the copper.

Table 1. The 2s2p multi-layer thermal model data set

nl_i	t_i [mm]	$\phi_{j,i}$ [%]	$ke_{j,i}$ [Wm^{-1}K^{-1}] (eq. 19)	$ke_{j,i}$ [Wm^{-1}K^{-1}] (eq. 20)
7	0.050	15	60.3	0.544
6	0.250	0	0.3	0.3
5	0.035	95	380	370
4	0.930	0	0.3	0.3
3	0.035	95	380	370
2	0.250	0	0.3	0.3
1	0.050	15	60.3	0.544

These results show that PCB heat-spreading capabilities depend mainly on both buried power-ground planes (3-5) of board structure.

Calculation corner

Mathcad® software version 15.0 was used to conduct the analytical model calculations. Its results are defined by the subscript AM, for analytical model calculation. To check the performances of the developed analytical model, a set of test cases is compared to the computations given by two electronic cooling software named Icepak® 15.0 (CFD1) and Flotherm® 9.3 (CFD2) as well as for special cases to ANSYS thermal (CFD3). The subscript NM for numerical model computation designs their results.

Pertinence of the analytical approach

At first, the purpose is to check its agreement to predict the thermal behavior of each layer of a complex board layout. Both models of effective thermal conductivities calculation are compared as well. The model was submitted to the following laboratory boundary conditions: both upper and lower heat transfer coefficients (ht, hr) at 12.2 W/m^{2}K, a reference temperature fixed at T_∞ = 85 °C, a square source of 5 mm with its centroid located at (37.5, 55, 1.6) mm, an uniform source dissipation of 0.5 W, upper limit values of truncated Fourier series are fixed at M = 225 and N = 300. In practice, the number of terms in the double summation is based on

a ratio proportional to a board size – source size which has to be multiply per an appropriate factor, named "a". In the current case, the "a" parameter has been fixed equal to 15:

$$M = a\frac{Lb}{Ls} \quad \text{and} \quad N = a\frac{Wb}{Ws} \tag{21}$$

The comparison of the models is done on the local and average temperatures of each board layer considering the planar source location and size. For small sources, this peculiar zone is the most sensitive path for heat spreading throughout the board. Two specific error metrics named ΔT_s and $\overline{\Delta T_S}$ are used to compare the models agreement, as reported in eq. 22. The numerical results are considered as the reference value:

$$\Delta T_s = \frac{T_{AM} - T_{NM}}{T_{NM} - T_\infty} \quad \text{or} \quad \overline{\Delta T_s} = \frac{\overline{T_{AM}} - \overline{T_{NM}}}{\overline{T_{NM}} - T_\infty} \tag{22}$$

Upper bound model

Table 2 presents the set of results for the studied seven-layer structure and the good agreement that is reached from the proposed analytical approach and both numerical simulations. Two distinct numerical models were created in order to confirm the numerical results.

Table 2. Cross-plane temperatures of a 2s2p board using upper bound model

	MATHCAD		CFD1				CFD2			
Layer location	Tc_{AM} [ºC]	Tav_{AM} [ºC]	Tc_{NM} [ºC]	Tav_{NM} [ºC]	ΔT_S [%]	$\overline{\Delta T_S}$ [%]	Tc_{NM} [ºC]	Tav_{NM} [ºC]	ΔT_S [%]	$\overline{\Delta T_S}$ [%]
z_7	104.8	101.8	104.8	101.9	0.1	0.3	104.8	101.9	0.2	–0.1
z_6	104.8	101.8	104.8	101.9	0.1	0.3	104.8	101.8	0.3	–0.1
z_5	95.2	94.5	95.1	94.4	–0.4	–0.6	95.1	94.4	0.4	0.3
z_4	95.2	94.5	95.1	94.4	–0.4	–0.6	95.1	94.4	0.4	0.2
z_3	90.5	90.5	90.6	90.4	0.1	–0.7	90.5	90.4	0.3	0.2
z_2	90.5	90.5	90.6	90.4	0.1	–0.7	90.5	90.4	0.3	0.2
z_1	90.3	90.2	90.3	90.3	0.1	–0.2	90.3	90.2	0.3	0.2
z_0	90.3	90.2	90.3	90.3	0.1	–0.2	90.3	90.2	0.3	0.2

The error percentage never exceeds 1% and the maximum temperature divergence is lower than 0.5 °C.

Lower bound model

Table 3 details the temperatures of the seven-layer structure when a pessimistic model of thermal conductivity calculation is used.

The error percentage remains below 1% and the maximum temperature divergence is lower than 0.5 °C. The high accuracy of the promoted analytical approach is resulting of the large number of the upper limits M and N of truncated Fourier series, chosen for the analysis. The comparison of the two tables demonstrates the impact of the choice of upper or lower bound model on the layer temperatures. Using lower bound model, the temperature of the heating source rises of more than 25% corresponding to temperature excess of 12 °C.Thus an optimistic calculation of effective thermal conductivities is going to significantly undervalue the maximum temperature encountered at the bottom side of the electronic component. The lower bound model is used in further calculations and its predictions are confronted to numerical simulations.

Table 3. Cross-plane temperatures of a 2s2p board using lower bound model

	MATHCAD		CFD1				CFD2			
Layer location	Tc_{AM} [ºC]	Tav_{AM} [ºC]	Tc_{NM} [ºC]	Tav_{NM} [ºC]	ΔT_S [%]	$\overline{\Delta T_S}$ [%]	Tc_{NM} [ºC]	Tav_{NM} [ºC]	ΔT_S [%]	$\overline{\Delta T_S}$ [%]
z_7	116.6	113.8	116.9	113.9	0.9	0.2	116.4	113.8	0.7	0.1
z_6	114.8	112.1	115.0	112.2	0.6	0.4	114.7	112.1	0.4	0.1
z_5	98.5	97.2	98.6	97.3	0.4	0.9	98.5	97.1	0.6	0.3
z_4	98.5	97.2	98.6	97.3	0.4	0.9	98.5	97.1	0.6	0.3
z_3	91.6	91.5	91.7	91.5	0.2	0.7	91.6	91.5	0.4	0.1
z_2	91.6	91.5	91.7	91.5	0.2	0.7	91.6	91.5	0.4	0.1
z_1	91.5	91.4	91.6	91.5	0.2	0.6	91.5	91.4	0.4	0.3
z_0	91.5	91.4	91.6	91.5	0.2	0.7	91.5	91.4	0.7	0.1

Industrial PCB layer layout

Multiple layers PCB with 4 to 16 copper trace layers have become the norm so the analytical model has to be able to quickly estimate the temperature of a heating source on such stack-up architectures.

Table 4. Example of a layer layout of an industrial PCB

nl_i	t_i [mm]	$\phi_{j,i}$ [%]	$ke_{j,i}$ [Wm^{-1}K^{-1}]
1-19	0.050	20	0.745
2-18	0.145	0	0.3
3-9-11-17	0.035	80	280
4-8-12-16	0.150	0	0.3
5-7-13-15	0.035	20	0.745
6-14	0.095	0	0.3
10	0.140	0	0.3

Thus a board structure of 10 copper trace layers, described in tab. 4, has been computed with the aim to evaluate the consuming time to analyze complex board architectures. The board is made of a symmetrical frame of 6 signal traces (1-5-7-13-15-19) and 4 internal copper planes (3-9-11-17).

Table 5 displays the result agreement for a source power of 0.5 W at laboratory boundary conditions.

Table 5. Temperature evaluation of a realistic PCB of 19 layers

	MATHCAD		CFD1				CFD2			
Layer location	Tc_{AM} [ºC]	Tav_{AM} [ºC]	Tc_{NM} [ºC]	Tav_{NM} [ºC]	ΔT_{DC} [%]	$\overline{\Delta T_{DC}}$ [%]	Tc_{NM} [ºC]	Tav_{NM} [ºC]	ΔT_{DC} [%]	$\overline{\Delta T_{DC}}$ [%]
5×5	109.2	106.9	109.2	106.9	0.1	–0.4	109.1	107.0	0.1	–0.4

For a compound electronic board of nineteen sandwiched layers, it can be seen that the maximum error is inferior to 1% and that temperature divergence never exceeds 0.5 °C. Moreover, the computation time has been compared between analytical and numerical calculation. Thus the determination of each selected point or area of the board using Mathcad® software can be run in 30 seconds. The vector of the source centered temperatures is computed is less than 25 minutes. At the opposite, the solving of all nodes of the numerical model is achieved in less than 3 hours.

Compact model of multi-layered PCB

It is generally assumed that a multi-layered PCB can be always efficiently represented by one homogenous layer having a couple orthotropic thermal conductivities and similar overall dimensions. If that assumption has the immediate benefit to permit shorter computation time, its influence on temperature prediction is often unknown in particular for small source, our primary concern.

Figure 3 presents the practical concept of a "compact" thermal modeling (CTM) of the board layer layout which is usually applied to an industrial electronic board.

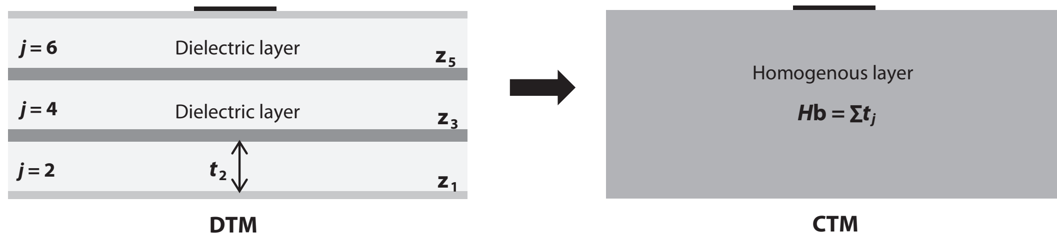

Figure 3. Reduction order of multi-layered PCB structure

As a useful technique [5], its in-parallel (the x- and y-directions) and in-series (the z-direction) effective thermal conductivities are calculated according to formula:

Stack-up of in-series n layers

$$\Rightarrow\ Rs = \sum_{i=1}^{n} Re_i \ \Rightarrow\ kz = \frac{\sum_{i=1}^{n} t_i}{\sum_{i=1}^{n} \frac{t_i}{ke_{z,i}}} \tag{23}$$

Stack-up of in-parallel n layers

$$\Rightarrow\ \frac{1}{Rp} = \sum_{i=1}^{n} \frac{1}{Re_i} \ \Rightarrow\ kx = \frac{\sum_{i=1}^{n} t_i \cdot ke_{x,i}}{\sum_{i=1}^{n} t_i} \ \text{ and } \ ky = \frac{\sum_{i=1}^{n} t_i \cdot ke_{y,i}}{\sum_{i=1}^{n} t_i} \tag{24}$$

For two-constituent layer, using in-plane and cross-plane stack-up expressions, the deducted thermal conductivities are, respectively:

- $kx = ky = 20.7$ W/mK and $kz = 0.336$ W/mK for upper bound model and
- $kx = ky = 16.5$ W/mK and $kz = 0.323$ W/mK for lower bound one.

As mentioned earlier, these sets of effective thermal conductivities demonstrate that an electronic board is strongly anisotropic. Thus the lower bound model promotes a reduced PCB efficiency to spread the heat in-plane, in peculiar for the closest layer of the heating source.

Table 6 show the comparison of the source temperatures for a multi-layered board and a single homogenous layer. The result confrontation is done for previous conditions and the lower bound model is used for the calculations of the effective thermal conductivities.

All displayed tables highlight the fact that the conventional practice for modeling PCB has to be carefully handled when the source size is going very small. The compact model returns a significant under evaluation of the temperature of the heating source.

Analytical model for board embedded sources

When a heating source is located at the interface of the s layer and $s + 1$ layer ($z = z_s$), the generalized steady-state governing equation need be solved for a new set of boundary conditions. Updated interlayer temperature continuity and flux conversion boundary conditions, for $0 \le x \le L_b$ and $0 \le y \le W_b$:

Table 6. Comparison of DTM-CTM predictions of the source temperatures

	(a) Using Mathcad						(b) From CFD1 software					
	DTM		CTM				DTM		CTM			
Source (mm2)	Tc_{AM} [ºC]	Tav_{AM} [ºC]	Tc_{AM} [ºC]	Tav_{AM} [ºC]	ΔT_{DC} [%]	$\overline{\Delta T_{DC}}$ [%]	Tc_{NM} [ºC]	Tav_{NM} [ºC]	Tc_{NM} [ºC]	Tav_{NM} [ºC]	ΔT_{DC} [%]	$\overline{\Delta T_{DC}}$ [%]
2.5×2.5	174.6	162.7	135.2	127.6	–44.0	–45.2	175.7	163.1	135.6	127.8	–44.3	–45.2
5×5	116.6	113.8	111.0	107.2	–17.7	–22.9	116.9	113.9	111.3	107.6	–17.6	–21.9
10×10	99.4	98.1	99.0	97.1	–2.8	–7.6	99.9	98.5	99.4	97.4	–3.2	–7.9

	c) From CFD2 software					
	DTM		CTM			
Source (mm2)	Tc_{NM} [ºC]	Tav_{NM} [ºC]	Tc_{NM} [ºC]	Tav_{NM} [ºC]	ΔT_{DC} [%]	$\overline{\Delta T_{DC}}$ [%]
2.5×2.5	172.3	161.6	135.0	127.7	–42.6	–44.0
5×5	116.4	113.8	110.7	107.2	–18.1	–22.9
10×10	99.3	98.0	98.7	97.0	–4.2	–8.1

$$\theta_{s+1}(x,y,z)\Big|_{z=z_s} = \theta_s(x,y,z)\Big|_{z=z_s} \tag{25}$$

$$kz_{s+1}\frac{\delta\theta_{s+1}(x,y,z)}{\delta z}\Bigg|_{z=z_s} - kz_s\frac{\delta\theta_s(x,y,z)}{\delta z}\Bigg|_{z=z_s} = e(x,y) \tag{26}$$

where $e(x, y)$ is the prescribed heat flux function at the common interface of adjacent layer.

The final solution forms of the temperature distribution are similar to previous expressions, only $\omega_{m,n,i}(z)$ has to be replaced by:

$$\begin{aligned} &0 \le z \le z_s \quad \Rightarrow \omega e_{m,n,i}(z) = \frac{Ner_{m,n,i}}{Der_{m,n,i}}\left[\omega c_{m,n,i}(z - z_{i-1}) + \frac{\chi u_{m,n,i}}{kz_i}\omega s_{m,n,i}(z - z_{i-1})\right]\mathrm{e}^{(z-Hb)r_{m,n,i}} \\ &z_s \le z \le Hb \Rightarrow \omega e_{m,n,i}(z) = \frac{Neu_{m,n,i}}{Deu_{m,n,i}}\left[\omega c_{m,n,i}(z_i - z) + \frac{\chi r_{m,n,i}}{kz_i}\omega s_{m,n,i}(z_i - z)\right]\mathrm{e}^{-(z+Hb)r_{m,n,i}} \end{aligned} \tag{27}$$

For a random set of interlayer sources (first column of tab. 7) a comparison of analytical and numerical models was led for the extreme boundary conditions. Table 7 presents the new temperatures mapping that is resulting of the evolution of internal boundary conditions (Neumann). The test is performed for an upper square source of 5 mm dissipating 0.5 W.

The prediction of the layer temperatures remains quite relevant and compliant with accuracy rules for early analysis of board design.

Cooling gain using thermal via matrix

Design of electronic board demands more and more the definition of practical modeling process to quickly evaluate the potential decrease of component temperature of multi-layer PCB such as thermal via structures use. Conventional PCB thermal attachment of electronic component pad is made of a matrix of plated through hole (PTH) via, having a diameter (D) of 0.3 mm at usually 1 mm pitch. Via drilled holes are electroplated with a minimum of 25 μm copper thickness (δv) throughout via barrel.

Figure 4 pictures the additional implementation of thermal via lands that is commonly made to extent it to direct thermal attachment of component pad to power-ground planes.

A full copper land pad is considered rightly beneath the heating source, its thermal conductivity is fixed at 400 W/mK. The dielectric substance is assumed to fill the remaining hole.

The comparison of tab. 3, and tab. 8 results allow to quantify the efficiency of a thermal via matrix to limit the source temperature.

Table 7. Impact of embedded sources on cross-plane temperatures

		MATHCAD		CFD1			
Q_i [W]	Layer location	Tc_{AM} [ºC]	Tav_{AM} [ºC]	Tc_{NM} [ºC]	Tav_{NM} [ºC]	ΔT_S [%]	$\overline{\Delta T_S}$ [%]
0.5	z_7	100.4	99.3	100.8	99.4	–2.3	–1.0
–0.429	z_6	98.7	97.5	99.0	97.7	–2.1	–1.6
0.429	z_5	96.6	95.6	96.6	95.6	–0.4	–0.4
–0.150	z_4	96.6	95.6	96.6	95.6	–0.4	–0.4
0.150	z_3	93.8	93.3	93.7	93.2	0.8	0.8
–0.0031	z_2	93.8	93.3	93.7	93.2	0.8	0.8
0.0031	z_1	93.8	93.3	93.6	93.1	1.7	1.7
0	z_0	93.8	93.3	93.6	93.1	1.5	1.6

Numerous experiments have demonstrated that thermal via land has major impact on the junction-to-ambient thermal resistance [10].

This JESD51-2's specific metrix of the thermal behavior of the chip is defined by:

$$R_{JA} = \frac{T_J - T_A}{Q} \tag{28}$$

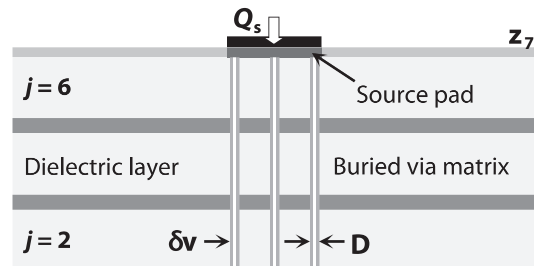

Figure 4. Common practice for draining component heat from thermal PTH vias

Its value indicates the sinking capacity of the total heating power (Q) of the device through all the thermal paths between chip junction (T_J) and ambient air (T_A). In the spotted case, the source-to-ambient thermal resistance decreases from 63.8 °C/W to 21.8 °C/W (CFD1) and proves the gain of thermal via clusters to limit excessive temperature. The center temperature of source is efficiently reduced of 20 °C. Moreover, the analysis of each layer temperature permits to identify the heat spreading effect of the various stacked via clusters. Therefore the board temperatures in source vicinity are more homogenous and its external opposite surfaces (0-7) are practically submitted to similar constraints.

Table 8. Cross-plane temperatures of a 2s2p board using a 5 × 5 thermal via matrix

	CFD1		CFD3	
Layer location	Tc_{NM} [°C]	Tav_{NM} [°C]	Tc_{NM} [°C]	Tav_{NM} [°C]
z_7	95,9	95,7	95,9	95,7
z_6	95,9	95,7	95,9	95,7
z_5	95,5	94,9	95,4	94,8
z_4	95,5	94,9	95,4	94,8
z_3	94,6	94,0	94,6	93,9
z_2	94,6	94,0	94,6	93,9
z_1	94,5	94,0	94,5	93,9
z_0	94,5	93,9	94,5	93,8

Effective thermal conductivity of thermal via areas

The previous fine modeling of the thermal via matrix is commonly substituted by a set of equivalent slabs having specific cross-plane thermal conductivities. The calculation of effective thermal conductivity of PTH via matrix is based on simple network of in series and in parallel thermal resistors. For this application case, the conventional linear rule of mixture model can be applied to determine the thermal properties of a continuous cross-plane structure of aligned thermal via which are buried in dielectric layers.

The following relationship formalizes the influence of a matrix of via on the cross--plane thermal conductivity of a simple epoxy resin slab. This last one takes into account the parallel heat spreading of a counted set of dielectric and annealed copper cylinders:

$$kvz = kr + \left(kv - kr\right)\frac{nv\,\pi\,\delta v\left(D - \delta v\right)}{LsWs} \tag{29}$$

Moreover, the number (nv), the pitch and size of thermal via must be chosen wisely to avoid making some of them useless to spread the heat in the high conductive planes of the board (3-5). Thus considering the defined parameters (D, δv), previous copper and dielectric thermal conductivities and a source square size of 5 mm, the cross-plane effective thermal conductivity of the homogenous slab is going to be equal to 2, 3.4, and 8.9 W/mK, when via numbers are 5, 9, and 25, respectively.

Practical analytical approach for modeling via clusters impact

This section describes a proposed analytical approach for modeling the influence of a local set of slabs having specific cross-plane thermal conductivities.

The principle is based on the appliance of appropriate set of positive and negative fictive sources that has been described previously. These ones are applied to the upper and lower interface where the slab is inserted. Figure 5 pictures the additional implementation of the initial analytical model that is defined with the purpose to extent it to direct thermal attachment of component pad to power-ground planes.

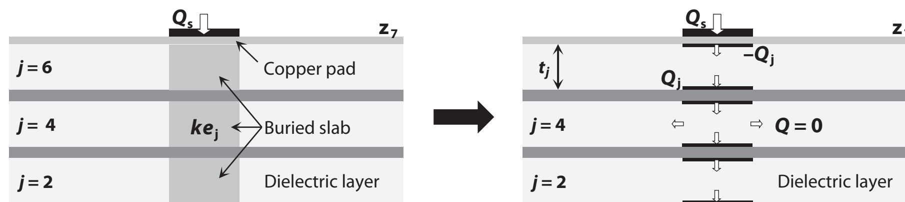

Figure 5. Concept of analytical modelling of multi-layered localized isotropic cuboid

The main assumption considers that due to very low thermal conductivity of the dielectric layers, 0.3 W/mK, the in-plane conduction is negligible. So the cross-plane heat flow rate through each slab is supposed constant.

By successive iterations a process flow permits to determine a vector of appropriate fictive dissipation that matches the interlayer thermal resistances on each thermal resistance of the set of modified cubes.

The fitting criterion for an isotropic slab inserted between z_j and z_{j-1} is given by:

$$[Rv_{i,j} + (Rx_{j,j} - Rx_{j-1,j})]Qv_j + Rx_{i,j}Q_i \to 0 \quad \text{where} \quad Rv_{i,j} = \frac{z_j - z_{j-1}}{kvz_j Ls_i Ws_i} \tag{30}$$

$$Rx_{i,j} = \sum_{m=0}^{M}\sum_{n=0}^{N} A_{m,i}B_{n,i}\overline{A_{m,i}}\;\overline{B_{n,i}}[\omega_{m,n,i}(z_j) - \omega_{m,n,i}(z_{j-1})] \tag{31}$$

The comparison of the novel analytical approach to numerical computation of multi-slab model is done for the following conditions: a full copper pad beneath the heating source with an isotropic thermal conductivity of 400 W/mK, three source-size slabs are taken into

account in the dielectric layers (2-4-6), their cross-plane thermal conductivity is fixed at 8.9 W/mK corresponding to a 5 × 5 matrix of thermal via, their in-plane thermal conductivity is assumed to be 0.3 W/mK.

Table 9 shows the board behavior when a direct thermal attachment of the source to both copper planes (3-5) is considered. Besides tab. 9 demonstrates that the slab of the layer 2 has a very poor impact on the source heat transfer to PCB structure and can be neglected to accelerate the source temperature calculation. The results confirm the assumption of the weak influence of in-plane conduction of the low-conductivity dielectric layer of the board.

Table 9. Impact of source-size slabs on cross-plane temperatures

	MATHCAD			CFD1			
Layer location	Q_i [W]	Tc_{AM} [°C]	Tav_{AM} [°C]	Tc_{NM} [°C]	Tav_{NM} [°C]	ΔT_S [%]	$\overline{\Delta T_S}$ [%]
z_7	–0.496	96.2	95.3	95.7	95.4	4.8	–0.7
z_6	0.017	96.2	95.3	95.7	95.4	4.8	–0.7
z_5	0.479	95.7	94.8	95.3	94.8	3.6	0.3
z_4	–0.218	95.7	94.8	95.3	94.8	3.6	0.3
z_3	0.218	94.8	94.1	94.5	93.9	2.9	2.1
z_2	–0.0039	94.8	94.1	94.5	93.9	2.9	2.1
z_1	0.0039	94.8	94.1	94.5	93.9	2.8	2.0
z_0	0	94.8	94.1	94.5	93.9	2.7	1.9

The agreement of both models demonstrates that it seems possible to take into account the presence of various thermal conductivity areas in an analytical approach using a technique based on a set of buried heating sources.

Moreover the comparison of tab. 3, and tab. 9. the relevance of the practical analytical approach to accurately evaluate the temperature of the source for a realistic case. The predicted source-to-ambient thermal resistances are, respectively, 21.2 °C/W and 21.4 °C/W.

Eventually, the analytical model allows weighting quickly the potential gain of large via number, such as 25, in order to select appropriate set of thermal via clusters in source vicinity.

Using that practical approach, the electronic designers will be able to early analyze the limits of the power dissipation of miniaturized devices at laboratory conditions.

Conclusions

A developed analytical model has been applied to estimate the temperature distribution of each layer of a set of industrial board frame, as well as the thermal test vehicle recommended by the US JEDEC Standard JESD51-7 to characterize the thermal performances of electronic component. Numerous comparisons for a set of parameters have been done with electronics cooling software to evaluate the pertinence of an analytical model for rugged ambient conditions. The agreement of the analytical model appears quite relevant as well as according with industrial accuracy expected level. Besides, the presented work highlights the fact that the concept of Compact Thermal Model for PCB can be very erratic, in particular when the size of the source is below 5 millimeters. Further the optimization of the conductive paths from the sensitive thermal surfaces of the package to the PCB is mandatory for the long-term survival of the device. Therefore a novel practical technique is defined to quickly quantify the potential benefit of a set of via placed just under the land pad of electronic component. The proposed model allows a local modification of the effective thermal conductivity of dielectric or external signal layers in order to optimize the component heat spreading in the board structure, our permanent objective.

Nomenclature

A_m, B_n – Fourier coefficients, [–]
G – thermal conductance, [WK^{-1}]
ht, hr – heat transfer coefficient, [Wm^{-2}K^{-1}]
i – layer identification, [–]
j – heating source identification, [–]
ke – effective thermal conductivity, [Wm^{-1}K^{-1}]

kx, ky, kz – isotropic thermal conductivities, [$Wm^{-1}K^{-1}$]
L_b, W_b, H_b – PCB dimensions, [m]
L_s, W_s, H_s – source dimensions, [m]
M, N – Fourier series truncation limit, [–]
nl – layers numbers, [–]
ns – heating sources numbers, [–]
Q_s – heating power, heat flow rate of source, [W]
q_s – heat flux density of source, [Wm^{-2}]
R – thermal resistance, [KW^{-1}]
T – temperature, [K]
T_∞ – reference temperature, [K]
t – layer thickness, [m]
xc, yc – center location of heating source, [m]

Acronyms

CCAF – copper covering area factor
DTM – detailed thermal model
CTM – compact thermal model

Greek symbols

δ – Kronecker function
θ – temperature excesses, [$= T(x,y,z) - T_\infty$], [K]
ϕ – volume fraction of filler
ω – z-axis thermal profile

Reference

[1] Vintrou, S., *et al.*, Calculation and Analysis of Thermal Impedance of Microelectronic Structures from Analytical Models, *Solid-State Electronics*, *67* (2012), 1, pp. 45-52
[2] Lopes Costa, R., Vlassov, V., Evaluation of Inherent Uncertainties of the Homogeneous Effective Thermal Conductivity Approach in Modeling of Printed Circuit Boards for Space Applications, *Journal of Electronics Cooling and Thermal Control*, *3* (2013), 1, pp. 35-41
[3] Karayacoubain, P., *et al.*, Thermal Resistance Based Bounds for Effective Conductivity of Composite Thermal Interface Materials, *Proceedings,* 22nd IEEE Semiconductor Thermal Measurement and Management Symposium, Dallas, Tex., USA, 2006, Paper No. 1-4244-0154-2
[4] Kotetov, R., *et al.*, Thermal Behaviour of Epoxy Resin Filled with High Thermal Conductivity Nano-powders, *Proceedings,* IEEE Electrical Insulation Conference, Montreal, Canada, 2009
[5] Shabany, Y., Component Size and Effective Thermal Conductivity of Printed Circuit Board, *Proceedings*, 9th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, San Diego, Cal., USA, 2002
[6] Funk, N., *et al.*, A Semi-Analytical Method to Predict Printed Circuit Board Package Temperature, *IEEE Transaction on Components, Hybrids and Manufacturing Technology*, *15* (1992), 5, pp. 675-684
[7] Schacht, R., *et al.*, Modeling Guidelines and Non-Destructive Analysis for Thermal and Mechanical Behaviour of Via-Structures in Organic Boards, *Proceedings*, 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, Orlando, Fla, USA, 2008, 441-449
[8] Monier-Vinard, E., *et al.*, Analytical Thermal Modeling of Multi-Layered Active Embedded Chips into High Density Electronic Board, *Thermal Science*, *17* (2013), 3, pp. 695-706
[9] Devoe, J., Ortega, A., An Investigation of Board Level Effects on Compact Thermal Models of Electronic Chip Packages, *Proceedings*, 18th IEEE Semiconductor Thermal Measurement and Management Symposium, San Jose, Cal., USA, 2002, Paper No. 0-7803-5624-5
[10] Brizoux, M., *et al.*, Industrial PCB Development Using Embedded Passive and Active Discrete Chips Focused on Process and DfR, *Proceeding*, IPC APEX Conference, Las Vegas, Nev., USA, 2010
[11] Muzychka, S., *et al.*, Thermal Spreading Resistance and Heat Source Temperature in Compound Orthotropic Systems with Interfacial Resistance, *Proceedings*, IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, Vol. 3, No. 11, pp. 1826-1841
[12] Rinaldi, N., Generalized Image Method with Application to the Thermal Modeling of Power Devices and Circuits, *Proceedings*, IEEE Transactions on Electron Devices, 2002, Vol. 49, No. 4, pp. 679-686
[13] Muzychka, Y. S., *et al.*, Thermal Spreading Resistance of Eccentric Heat Sources on Rectangular Flux Channels, *Journal of Electronic Packaging*, 125, (2003), 2, pp. 178-185
[14] Culham, J. R., Yovanovich, M. M., Factors Affecting the Calculation of Effective Conductivity in Printed Circuit Boards, *Proceedings*, 6th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electric Systemes, Seattle, Wash., USA, 1998
[15] Muzychka, Y. S., *et al.*, Influence of Geometry and Edge Cooling on Thermal Spreading Resistance, *Journal of Thermophysics and Heat Transfer*, *20* (2006), 2, pp. 247-255

Appendix

$$r_{m,n,i} = \sqrt{\left(\frac{m\pi}{Lb}\right)^2 \frac{kx_i}{kz_i} + \left(\frac{n\pi}{Wb}\right)^2 \frac{ky_i}{kz_i}}$$

$$\omega c_{m,n,i}(z) = 1 + e^{-2zr_{m,n,i}} \quad \text{and} \quad \omega s_{m,n,i}(z) = \frac{1 - e^{-2zr_{m,n,i}}}{r_{m,n,i}}$$

$$\alpha_{m,n,i} = kz_i r_{m,n,i}{}^2 \omega s_{m,n,i}(t_i) \quad \text{and} \quad \beta_{m,n,i} = \frac{1}{kz_i}\omega s_{m,n,i}(t_i) \quad \text{and} \quad \gamma_{m,n,i} = \omega c_{m,n,i}(t_i)$$

$$Du_{m,n,i} = \alpha_{m,n,nl} + ht\,\chi u_{m,n,nl}\beta_{m,n,nl} + (\chi u_{m,n,nl} + ht)\gamma_{m,n,nl}$$

$$Nu_{m,n,i} = \frac{e^{r_{m,n,nl}(z_{nl-1} - Hb)}}{e^{r_{m,n,i}(z_{i-1} - Hb)}} \prod_{j=i}^{nl-1} \frac{2e^{-t_j r_{m,n,j}}}{\gamma_{m,n,j} + \chi u_{m,n,j}\beta_{m,n,j}}$$

$$Dr_{m,n,i} = \alpha_{m,n,1} + hb\,\chi l_{m,n,1}\beta_{m,n,1} + (\chi l_{m,n,1} + hb)\gamma_{m,n,1}$$

$$Nr_{m,n,i} = \frac{e^{-r_{m,n,1}z_1}}{e^{-r_{m,n,i}(z_i + Hb)}} \prod_{j=i}^{2} \frac{2e^{-t_j r_{m,n,j}}}{\gamma_{m,n,j} + \chi r_{m,n,j}\beta_{m,n,j}}$$

$$Der_{m,n,i} = (\chi u_{m,n,s+1} + \chi r_{m,n,s})(\gamma_{m,n,s} + \chi u_{m,n,s}\beta_{m,n,s})$$

$$Deu_{m,n,i} = (\chi u_{m,n,s+1} + \chi r_{m,n,s})(\gamma_{m,n,s+1} + \chi r_{m,n,s+1}\beta_{m,n,s+1})$$

$$Ner_{m,n,i} = \frac{e^{-r_{m,n,s}t_s}}{e^{r_{m,n,i}(z_{i-1} - Hb)}} \prod_{j=i}^{s-1} \frac{2e^{-t_j r_{m,n,j}}}{\gamma_{m,n,j} + \chi u_{m,n,j}\beta_{m,n,j}}$$

$$Neu_{m,n,i} = \frac{e^{-r_{m,n,s+1}t_{s+1}}}{e^{-r_{m,n,i}(z_i + Hb)}} \prod_{j=i}^{s+2} \frac{2e^{-t_j r_{m,n,j}}}{\gamma_{m,n,j} + \chi r_{m,n,j}\beta_{m,n,j}}$$

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