THERMAL ANALYSIS OF THE INFLUENCE OF CHIP ARRANGEMENT OF A WATER-COOLED MINICHANNEL HEAT SINK

by

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Electronic chips are arranged in various manners according to design conditions and constraints, and thus the influence of chip arrangement on the entire thermal performance should be understood ahead of design and manufacture of electronic cooling systems. In this paper, a minichannel heat sink is considered for electronic cooling, and three kinds of chip arrangement are designed and studied: diagonal arrangement (Case 1), parallel arrangement (Case 2), and stacked arrangement (Case 3). The single-phase laminar liquid flow and conjugated heat transfer of the minichannel heat sinks are investigated through computational fluid dynamics technique for dealing with the normal-scale Navier-Stokes equations and energy equations. Numerically predicted results are qualified by comparing the previous experimental data and by a grid-independent test. Temperature distributions on the chip surfaces are presented and the thermal performance in terms of total thermal resistance is also compared. It is found with diagonal arrangement (Case 1) the minichannel heat sink provides the best thermal performance.

Key words: *chip arrangement, thermal resistance, temperature, laminar flow*

Introduction

Electronic devices and systems are reduced gradually in size while a rapid growth in their functions and complexity has been encountered over the past four decades. This trend leads to increasingly high heat density generated by the electric current, and brings a challenge to the cooling techniques. How to prevent overheating is a critical issue in the compact design of electronics. To avoid any possible failure or malfunction of electronics and ensure the reliability of the electronic systems, it is essential to maintain the temperature of the electronic components below an acceptable upper limit. It is beyond the capability of traditional air-cooling techniques to remove a large amount of dispersed heat from a small space. Therefore, alternative methods with heat removal capabilities at least one order of magnitude larger than that of conventional ones become necessary.

Tuckerman and Pease [1] introduced a kind of water-cooled heat sink made of silicon, used in very-large-scale integrated circuits. The microchannels were fabricated with a 50 μm width and a 300 μm height so that heat fluxes as high as 790 W/cm^2 could be removed with the maximum temperature difference between substrate and inlet water of 71 K and the pressure drop across the micro-channels of 31 Pa. The thermal performance is much better

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than presented by conventional thermal dissipation technologies. After that, many researchers focused on such new kind of chip cooling technology. Kandlikar and Upadhye [2] and Kandlikar and Grande [3] did a series studies and reviews on the minichannels and microchannels liquid cooling technology. Schmidt [4] discussed the challenges in electronic cooling with microprocessor liquid cooled minichannel heat sink. Anandan and Ramalingam [5] addressed a review of thermal management of electronics and highlighted developments of new cooling methods. Venkatadri *et al.* [6] reviewed the recent advances in thermal management in 3-D chip stacks in electronic system, and discussed the 3-D integration technologies, thermal management challenges and advanced 2-D thermal management.

Wei and Joshi [7] numerically investigated the effects of channel aspect ratio and number of layers on stacked microchannel heat sinks. Xie *et al.* [8, 9] performed numerical studies on the laminar/turbulent flow and heat transfer characteristics of a water cooled straight minichannel heat sink. The results showed that heat flux could be removed from 256 W/cm^2 to 350 W/cm^2 for a nearly-optimized microchannel, and the pumping power increased from 0.205 W to 5.365 W as well. Steinke *et al.* [10] also developed an experimental facility for investigation of single-phase liquid flow in microchannels. Thermohydraulic performance of microchannels was studied as a function of channel geometry, heat flux, and liquid flowrate. Qu and Mudawer [11] analyzed heat transfer characteristics in a rectangular microchannel heat sink using water as cooling fluid. Cho *et al.* [12] simulated the flow distribution in microchannel heat sinks with non-uniform heat flux conditions. In order to investigate the effect of non-uniform heat flux, three different conditions over the channel area are evaluated and compared. Levac *et al.* [13] numerically analyzed the thermal performance of a double-layer microchannel under laminar flow condition, and compared the thermal performance for parallel-flow and counter-flow layouts at different Reynolds numbers. Manglik *et al.* [14] considered steady forced convection in wavy-plate fin channels at periodically developed low Reynolds number. The numerical results showed that counter-rotating vortices occurring in the wall-trough regions of the flow cross-section enhanced fluid mixing and leaded to improved heat transfer performance, but in lower wavy-fin density and Reynolds number, viscous forces may dominate and suppress or diminish the extent of swirl. Sivasankaran *et al.* [15] experimentally studied of parallel plate and crosscut pin-fin heat sinks, and found that the parallel plate heat sink provided higher averaged heat transfer coefficient than the pin-fin heat sink. Recently, Arif *et al.* [16] performed thermal-structural analysis of the effect of thermal interface between the fin and base plate of pin-fin heat sinks as well as the effect of various interface geometrical and contact properties. Xie *et al.* [17, 18] also did computational studies about laminar heat transfer of double-layer and wavy microchannel heat sinks, and comparative comparisons were made on their thermal performance [19, 20].

Though there existed many studies on minichannels heat transfer characteristics, only one-branch minichannel channel was investigated because of symmetrical or periodical geometries under studied, and simplified constant heat flux condition was assumed for the overall bottom surface where the heating chips were bonded at some covering regions. In real engineering situations, electronic chips are always placed in various manners according to design conditions and constraints, in this case the assumption of uniform heat flux is acceptable for chips surfaces rather than for the entire bottom surface. Besides, it is expected that the arrangement of electronic chips has a certain effect on the entire thermal performance in terms of local maximum temperature (thereby the thermal resistance) and overall temperature uniformity. Therefore, it is necessary to perform overall simulations of the packaged minichannel with fluid and solid portions, and to observe the effects of chip placement on liquid cooling

performance so as to provide the useful information for the design of electronic cooling systems with integrated heat sinks.

Physical models

A schematic diagram of the geometrical models and the chip arrangement considered in this study are provided in figs. 1 and 2. There are 20 minichannels in this heat sink with bottom surface (heated by two chips) size of 35 mm $\times$35 mm. Three different kinds of chips arrangement are designed and studied. The size of chip is 15 mm $\times$15 mm. A simple notation is introduced as: Case 1 – diagonal arrangement, Case 2 – parallel arrangement, and Case 3 – stacked arrangement. The geometrical parameters of single minichannel in detail are: the wall thickness W_w = 0.75 mm, the channel width W_c = 1 mm, the channel height H_c = 4 mm; the cover plate thickness H_t = 0.5 mm (Case 1 and Case 2); the cover plate thickness H_t = 1 mm (Case 3); the substrate thickness H_s = 0.5 mm (Case 1 and Case 2); the substrate thickness H_s = 5 mm (Case 3). For Case 1, the distance between the chip and boundary is 2 mm, and the distance between the two ships is 1 mm. For Case 2, the left (right), front (back) distance between the chip and boundary is 10 mm and 2 mm, respectively. For Case 3, the distance for the first chip from the bottom is 3 mm, the distance for the second chip from the bottom is 1 mm, and the volume for chip is 15 mm$\times$15 mm$\times$1 mm.

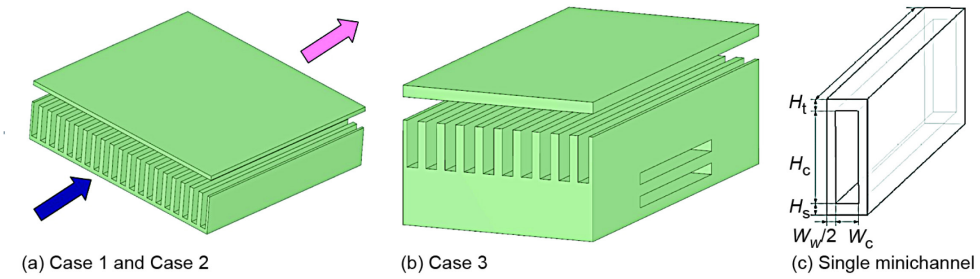

Figure 1. The heat sink configuration

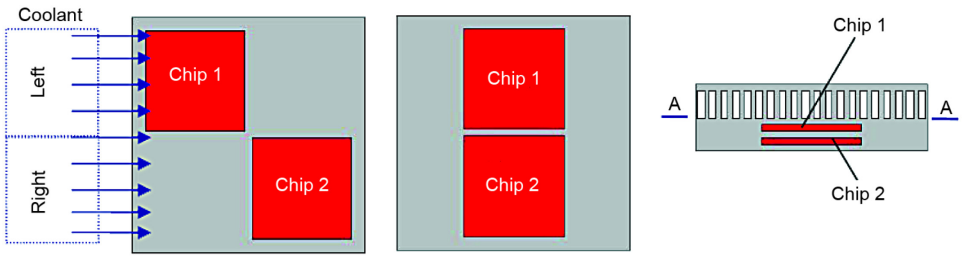

Figure 2. The different chips arrangement

Numerical details

Governing equations

The finite volume modelling was conducted by applying the simulation software FLUENT version 12.1. The flow and thermal characteristics of every minichannel for all cas-

es were evaluated and compared. For simplification of modelling simulation, the following assumptions were made:

– the flow is 3-D, incompressible, laminar and in steady-state,
– the effect of body force is neglected, and
– thermophysical properties of fluid and solid do not vary with temperature.

The governing equations for laminar flow and heat transfer are:

– mass equation

$$\frac{\partial(\rho u_{\mathrm{i}})}{\partial x_{\mathrm{i}}} = 0 \tag{1}$$

– momentum equation

$$\rho \frac{\partial(u_{\mathrm{i}} u_j)}{\partial x_{\mathrm{i}}} = -\frac{\partial p}{\partial x_{\mathrm{i}}} + \mu \frac{\partial^2 u_j}{\partial x_{\mathrm{i}}^2} \tag{2}$$

– energy equation

$$\rho \frac{\partial(u_{\mathrm{i}} T)}{\partial x_{\mathrm{i}}} = \frac{\lambda}{c_p} \frac{\partial^2 T}{\partial x_{\mathrm{i}}^2} \tag{3}$$

– Reynolds number is defined

$$\mathrm{Re} = \frac{\rho u_m D_{\mathrm{h}}}{\mu} \tag{4}$$

where ρ is the fluid density, u_m – the average velocity of fluid in the channel, which is equal with the inlet velocity, D_{h} – the hydraulic diameter, and μ – the dynamic viscosity.

To evaluate and compare the overall thermal performance of heat sink, the thermal resistance is defined:

$$R = \frac{T_{\max} - T_{\mathrm{in}}}{Q} \tag{5}$$

where $T_{\max}$ is the maximum temperature on the chip, T_{in} – the inlet fluid temperature and the value is 293.15K, and Q – the power generated by the chip and the value is 150 W.

The commercial software FLUENT is applied to solve the governing equations with appropriate boundary conditions. The pressure and velocity fields are handled by the semi-implicit method for pressure linked equations (SIMPLE) algorithm. The standard scheme is used for pressure discretization, while the second order upwind scheme is used for momentum and energy equations.

Boundary conditions

Due to the relatively high thermal conductivity of silicon, a uniform heat flux is applied on the heat-generating chip. Other walls of the heat sink are assumed to be adiabatic. Pressure outlet is selected at the outlet for the calculation of pressure drop across the channel. The initial temperature of coolant was assumed as 20 °C (293.15 K). No-slip boundary conditions are applied to all channel walls. The computations are considered to be converged when

the residues for all governing equations were less than $1 \cdot 10^{-6}$. In order to reduce the thermal stress between the heat sink and chip, silicon whose thermal conductivity is 148 W/mK, is chosen as the material of heat sink. It is helpful for improving the reliability of chips. In addition, water as the coolant is used to remove the heat load since it has high heat capability.

Grid independence

The accuracy of the simulation depends on the quality of the mesh. In general, a hexahedral mesh provides a more accurate solution than the tetrahedral mesh for the same conditions. Three different mesh number systems have been tested at a Re = 210, namely 1.5 M, 2.35 M, and 3 M for Case 1. The tested results are listed in tab. 1. It was found that the difference of pressure loss and thermal resistance for Case 2 are smaller than that of Case 1. For pressure loss, the deviation of Mesh I and Mesh II are 3.261% and 1.865%, respectively. The Mesh density has influence on thermal characteristics, *e. g.* the maximum deviation of thermal resistance is 0.929% for Mesh II, while it is 2.476% for Mesh 1. Thus, to keep a balance between computational economy and prediction accuracy, the meshes including 2.35 M and 3.7 M cells, are chosen for Case 1, Case 2, and Case 3, respectively.

Table 1. Grid independence study for Case I

	Mesh I (1.5 M)	Mesh II (2.35 M)	Mesh III (3 M)
Δp	72.10	73.14	74.53
R (chip 1)	0.315	0.326	0.323
R (chip 2)	0.337	0.343	0.344
Difference, [%]	3.261% 2.476% 2.035%	1.865% 0.929% 0.291%	baseline

Model validation

To validate the present computational method, the experimental model with a microchannel heat sink in [18] was adopted. Each microchannel had a width of 54 μm and a height of 215 μm. Figure 3 shows the comparison of temperature difference between the present simulated results and the experiment data, [21, tab. 6]. A good agreement was found with the experimental data. A maximum deviation of 6.9% in fluid temperature difference between inlet and outlet was found. Thus, the numerical model can be used with the acceptable engineering accuracy. In the present study, a laminar model was chosen to numerically investigate thermal characteristics over the Reynolds number range of 100-400.

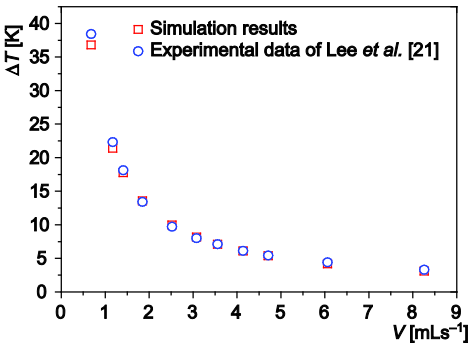

Figure 3. Comparison of temperature difference

Numerical results and discussion

The chips have different maximum temperatures and temperature distributions because of the different chip location on the heat sink bottom. Figure 4 shows the temperature contour of the six chip surfaces. It can be seen that the temperature near the peripheral boundary is lower than that in the central areas, and the spot of the maximum temperature is located in the rearward of chips. For the Case 1, the temperature of the second chip is higher than that of the

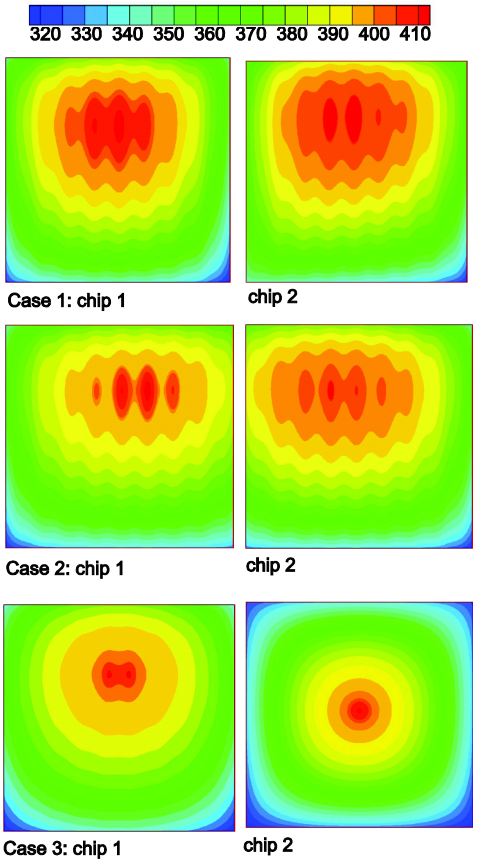

Figure 4. Chip temperature contour *(for color image see journal web-site)*

first chip, and its hot area is larger. But temperature distributions have almost the same trend (as shown in fig. 5). For the Case 2, the two chips have almost the same temperature distribution, but the highest temperature point of first chip is on the right side and that of the second chip is on the left side. For the Case 3, the first chip has better temperature distribution than the second chip, indicating that the heat generated by the second chip is only taken away a small extent. The chip may achieve very good cooling performance when the distance between two chips is increased and the chips are closer to the water-cooling minichannels. From the previous results, it suggests that a reasonable arrangement of the chips can obtain a good cooling performance when the minichannel heat sink has been designed in advance.

Figure 5 presents the temperature distribution of the chips at the different positions along with the flow direction. It can be clearly seen that the twelve profiles have the same trends along with the z-direction. The temperature is increased first and then reduced, and the highest temperature is near the back-sides (rearward). The temperature of Case 3-chip 2b is increased and then decreased severely.

The relationship between thermal resistance and Reynolds number is presented in fig. 6. The larger flowrate of the coolant through the cooling minichannels, the more thermal load generated by chips can be taken away. It can be seen from fig. 7 that the thermal resistance decreases with the increasing of the Reynolds number. It is also observed obviously that for the Case 1, chip 1 presents the least thermal resistance

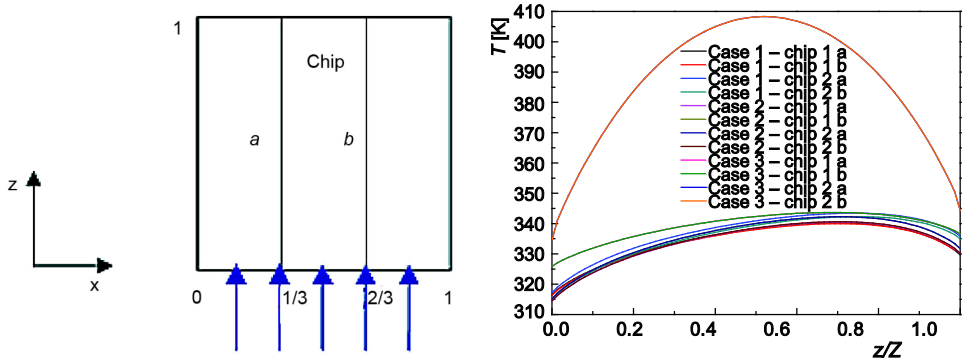

Figure 5. Chip temperature distribution along flow direction *(for color image see journal web-site)*

at all Reynolds numbers and thereby has the best cooling effectiveness, whilst chip 2 has a little higher thermal resistance. This is reasonable because the coolant in the left-side (as shown in fig. 2) first flows through the minichannels above the chip 1 and thus the cooling potential of the coolant is fully utilized, whereas the right-side coolant flows through the regions without chip and later through the minichannels above the chip 2. Besides, the temperature in the right side is slightly increased along with the flow direction from the inlet due to the transversal heat conduction from the heat generated by the chip 1, as shown in fig. 7.

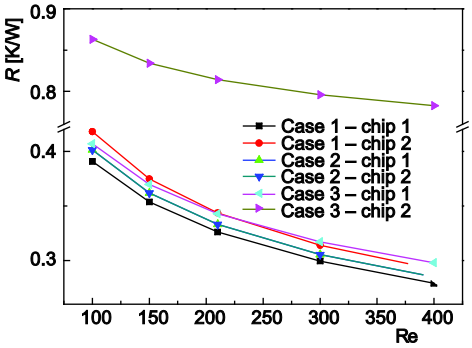

Figure 6. Thermal resistance with Reynolds number *(for color image see journal web-site)*

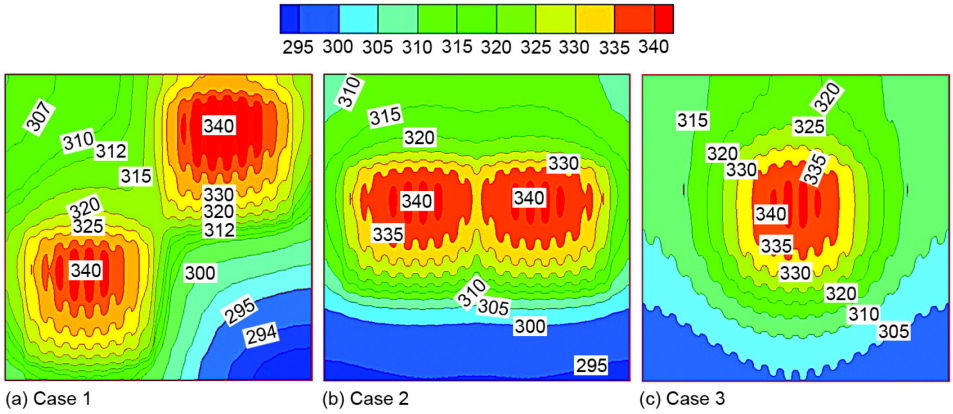

Figure 7. Temperature distribution on bottom surfaces *(for color image see journal web-site)*

For the Case 2, the two chips have almost the same thermal resistance, but are slightly larger than that of Case 1, chip 1. This is because only the coolant inside the central minichannels is used to cool the two chips. For the Case 3, the two chips have the different situation. The first chip has the much lower thermal resistance, implying the better cooling effect, whilst the second chip has the very higher thermal resistance and the cooling effect is extremely bad. This may be because that the chip 1 is very near the cooling minichannels and thereby the convective cooling impact between the coolant and substrate is mainly dominative, while the heat conduction inside the substrate is mainly dominative and the impact of convective cooling may be less.

The sliced temperature distributions of Case 1 and Case 2 are shown in fig. 8. It can be seen that the chip arrangement obviously affects the 3-D temperature distribution. Similar, for Case 1, the low temperature region is found near the inlet part where the chip is far away, and for Case 2 the distribution is symmetrical but with slightly higher value of temperature at the same section. From the previous results, it is suggested that with a reasonable arrangement of the chips, one can obtain a good cooling performance when the minichannel heat sink has been designed in advance.

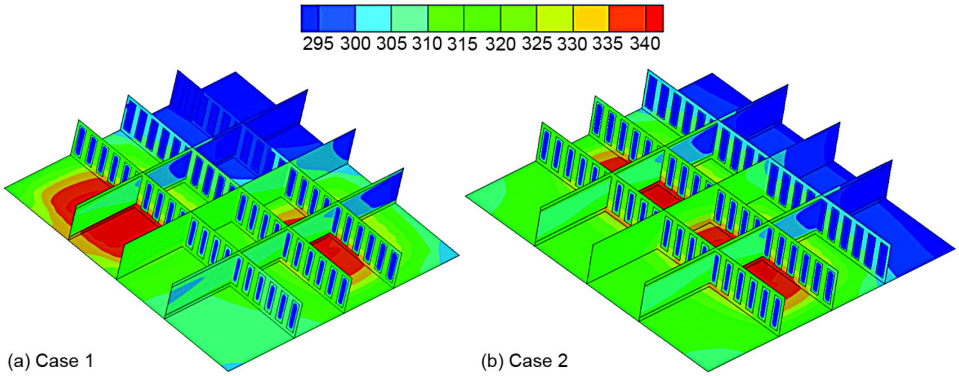

Figure 8. Slice temperature distribution *(for color image see journal web-site)*

Conclusions

Minichannel heat sink is an attractive way to cool electronic chips. In this study, 3-D simulations of the laminar heat transfer in a water-cooled minichannels heat sink with various chip arrangements were performed by CFD approach. To observe the effect of electronic chips arrangement, three cases were considered. The results indicate that the arrangement of chips would affect the chip surface temperature and thus the thermal performance. There are hot spots on the chip surface, and the temperature distribution on the chip wall is non-uniform. The highest temperature of one of the diagonal arrangement chips is the least among the three cases. For the stacked arrangement chips, the second chip may burn for the very high temperature on the chip center. It is suggested that a reasonable chips arrangement can remove more heat loads and thus achieve a good cooling performance.

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Nomenclature

c_p – specific heat, [Jkg^{-1}K^{-1}]
D_h – hydraulic diameter, [m]
H – height, [m]
Q – power generated by the chip, [W]
R – thermal resistance, [KW^{-1}]
Re – Reynolds number, (= $\rho u_m D_h/\mu$), [–]
T – temperature, [K]
u – flow velocity, [ms^{-1}]
v – volumetric flow rate, [mLs^{-1}]
W – width, [m]

Greek symbols

μ – fluid dynamic viscosity, [Pa·s]
λ – thermal conductivity, [Wm^{-1}K^{-1}]
ρ – fluid density, [kgm^{-3}]

Subscripts

c – microchannel
s – substrate
t – top cover
in – inlet
max – maximum
w – wall

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